E C S

Electronic Components and Systems

Micro-nano electronics challenges in KDT

Workshop 27/05/2021

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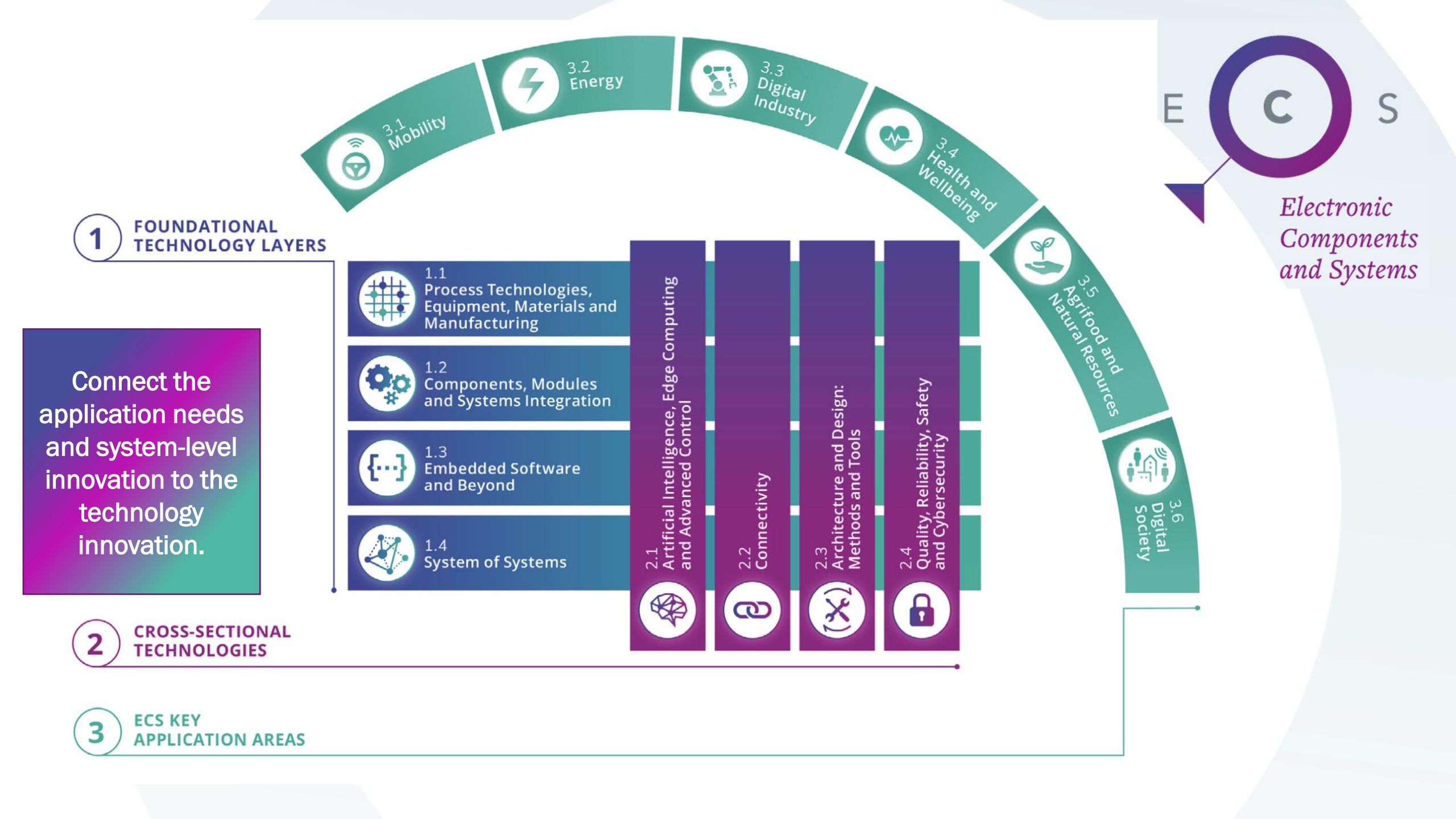
CSO & EVP imec


3.1 Mobility
3.2 Energy
3.3 Digital Industry
3.4 Health and Wellbeing
3.5 Agrifood and Natural Resources
3.6 Digital Society
1 FOUNDATIONAL TECHNOLOGY LAYERS
1.1 Process Technologies, Equipment, Materials and Manufacturing
1.2 Components, Modules and Systems Integration
1.3 Embedded Software and Beyond
1.4 System of Systems
2.1 Artificial Intelligence, Edge Computing and Advanced Control
2.2 Connectivity
2.3 Architecture and Design: Methods and Tools
2.4 Quality, Reliability, Safety and Cybersecurity
2 CROSS-SECTIONAL TECHNOLOGIES
3 ECS KEY APPLICATION AREAS
Connect the application needs and system-level innovation to the technology innovation.
E C S
Electronic Components and Systems

EU Main Objectives taken up by SRIA

Electronic Components and Systems

- Boost industrial competitiveness through interdisciplinary technology innovations
- Ensure European digital autonomy through secure, safe and reliable ECS supporting key European application domains
- Establish and strengthen sustainable and resilient ECS value chains supporting the Green Deal
- Unleash the full potential of intelligent and autonomous ECS-based systems for the European Digital Age

Timeline

MILESTONES TO BE REACHED VIA COLLABORATIVE RESEARCH PROJECTS ACROSS EUROPE

SHORT TERM (2021–2025)	MEDIUM TERM (2026–2030)	LONG TERM (2031 AND BEYOND)

Industrial competitiveness

- Additive manufacturing, rapid prototyping
- Modular multi-application architecture supporting AI and advanced sensing and control
- Remote engineering and operations, telepresence
- Advanced human-machine joint intelligence
- Time-critical functions moved to the cloud
- Cost- and effort-effective, continuous virtual ECS development and validation processes
- Zero defect design and manufacturing and circular economy for ECS
- Certified trusted hardware and embedded software for autonomous systems

EU sovereignty

- EU devices enabling 5G connectivity
- Leveraging open source or alternatives to develop advanced European AI edge solutions
- 6G connectivity RF and photonics devices
- New self-learning methods to ensure safe operations of complex systems
- End-to-end AI-based security
- 1 nm node semiconductor equipment
- EU ecosystems for dependable SW
- Trustable AI-based IoT systems
- Quantum and other novel paradigm technologies for computing, communication and sensing

Sustainability and Green Deal

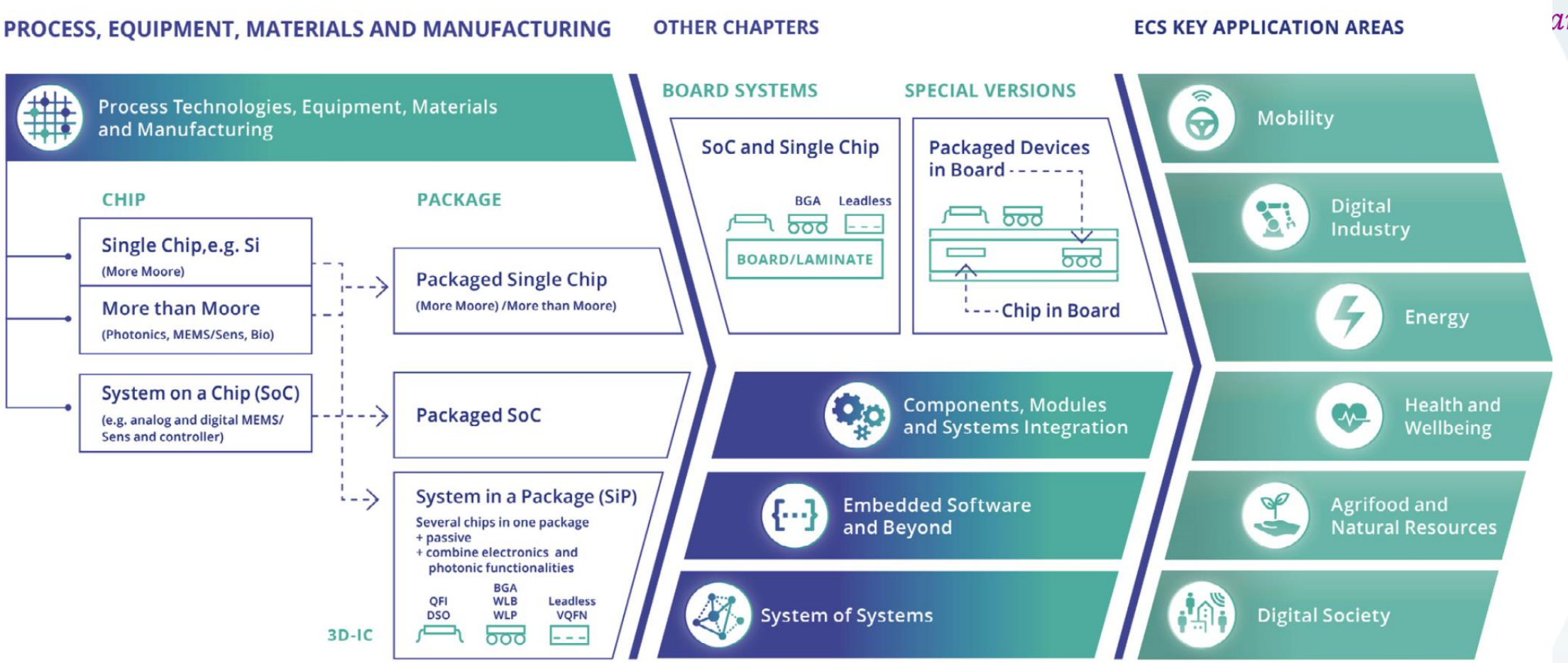
- Materials enabling recycling and repair
- Supply-chain aware design flows
- Energy-optimised EV urban mobility
- New Power devices
- Energy management towards tow/zero power
- Energy-optimised H_2 long-distance mobility
- Food Traceability over the whole value chain
- Organic, compostable and biodegradable materials
- Emission-free cities
- From cradle to grave CO_2-neutral mobility
- Reduction of cumulated carbon and cultivated land footprint by 20% in the next 20 years

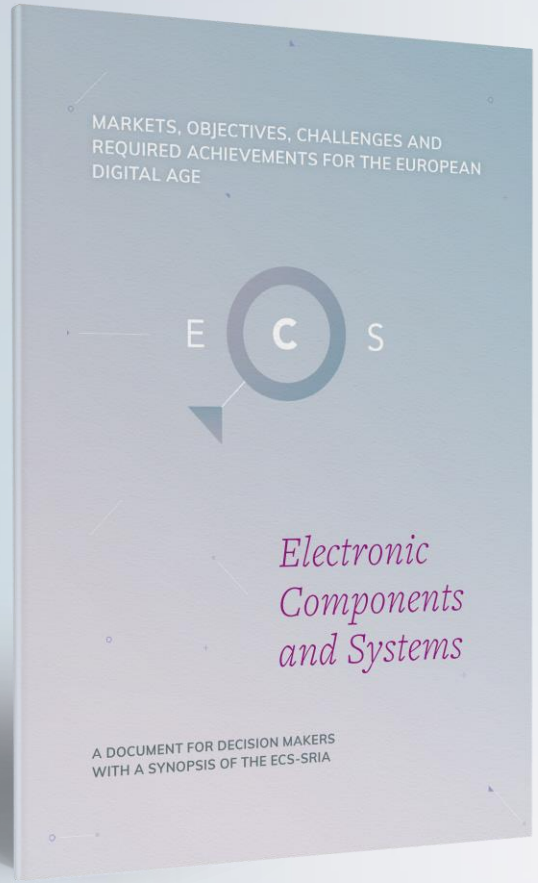
Europe's Digital Age

- Communication infrastructure to support self-organised communities
- IoT-based health care solutions
- Sensing and processing for clean, connected and automated vehicles
- Improved and new human-machine interfaces
- Next-generation (patch-like) drug delivery systems part of the Internet of Medical Things
- Validation and certification procedere for clean, connected and automated vehicles
- Real-time emotion sensing
- Organ-on-a-chip developments addressing rare diseases
- Instant information understanding between systems

The SRIA reference frame

Electronic Components and Systems





Micro-nano electronics challenges

Focus areas for this workshop

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Major challenge 1: Advanced computing, memory and in-memory computing concepts

Electronic Components and Systems

Scope

Semiconductor process technology and integration actions will focus on the introduction of ***new materials, devices and concepts****, in close collaboration with the* ***equipment, materials, modelling/simulation and embedded software communities****, to allow for the necessary* ***diversity in computing infrastructure****.*

The applications range ***from high-performance*** *cloud/edge computing in servers, office/home computing, mobile computing, and* ***ultra-low power data processing at the IoT node*** *level up to the highest possible performance.*

Expected achievement

Maintaining competence on advanced logic and memory technology in Europe is key to maintaining sovereignty and supporting societal benefits from the core technology base. Implementation of dedicated and sustainable pilot lines for specialised logic processes and devices supporting European critical applications is also a major objective, as is the exploration of new devices and architectures for low-power or harsh environment applications.

PRIORITY

Explorations of the scaled Si technology

3 nm node and beyond (including FDSOI, FinFET/Trigate and stacked gate-all-around horizontal or vertical nanowires, Forksheet, complementary FET architectures, 3D integration), and further device and pitch scaling where parallel conduction paths (nanowires, nanosheets, etc) are brought even closer

PRIORITY

Unconventional devices and materials

Exploration and implementation of materials beyond Si (SiGe, SiC, GaN, Ge, InGaAs, functional oxides, 2D material heterostructures, nanowires).
such as 2D and III-V materials, metamaterials, metasurfaces, nanowires, nanosheets, nanoparticles, quantum dots, spin effects, functional oxides, ferroelectric and magnetic, which are being investigated to overcome the limits of conventional CMOS logic and memories.

PRIORITY

Novel device, circuit and system concepts and novel paradigms

Optimum PPAC specifications, high-energy efficiency and novel paradigms such as for near/in-memory, neuromorphic, optical and quantum computing. Long-term challenges such as steep slope switches (tunnel FET, negative capacitance FET, nanoelectromechanical systems, NEMS), spin-based transistors, and alternative high- performance switches.

PRIORITY

Local AI processing and storage of data

New embedded non-volatile memory (eNVM) technologies to enable local AI processing and storage of configuration data, which decrease data transmission volume, energy needs and allow for more efficient control of electric powertrains and batteries.

Timeline

Advanced computing, memory and in-memory computing concepts

Electronic Components

MAJOR CHALLENGE	TOPIC	SHORT TERM (2021–2025)	MEDIUM TERM (2026–2029)	LONG TERM (2030–2035)
Major challenge 1: Advanced computing, memory and in-memory computing concepts	**Topic 1.1:** Extensions of the scaled Si technology roadmaps High-performance Ultra-low power 3D integration	• N3 - N2 R&D • 2nd generation gate-all-around devices, forksheet integration • 18 nm FDSOI at technology platform integration level	• N1,5 R&D - 3rd generation of Gate-All-Around devices • CFET introduction • 12/10 nm FDSOI at technology platform integration level • 3D monolithic integration	• Sub-1 nm node logic and memory technology (nanowires, nanosheets) at process and device research level • Vertically stacked nanosheets • 3D monolithic integration • Beyond 10 nm FDSOI at technology platform integration level
	Topic 1.2: Exploration and implementation of unconventional devices based on materials beyond Si	• SiGe (high Ge) channel • Cu alternative solutions	• Ge channel • Optical interconnects • 2D materials exploration	• III-V channel • 2D materials device integration
	Topic 1.3: Novel device, circuit and systems concepts, such as for near/in-memory, neuromorphic, optical and quantum computing neuromorphic, optical and quantum computing	• Near/in-memory computing • 3D heterogeneous integration (logic/memory)	• In-memory computing • Neuromorphic computing (spiking) • 3D monolithic integration • Photonic SOI	• Quantum computing • Optical computing
	Topic 1.4: Long-term challenges such as steep-slope switches, spin-based transistors and alternatives		• TFET • CNTFET • 2D material FET	• NCFET • NEMS switch • Topologic insulator electronic devices • Spin wave devices • Mott FET (VO_2, HfO_2, etc)
	Topic 1.5: New eNVM technologies	• PCRAM • STT-MRAM • FDSOI embedded MRAM	• PCRAM • VCMA-MRAM • ReRAM • FeRAM	• ReRAM (MLC) • Hi-density ReRAM

Major challenge 2: Novel devices and circuits that enable advanced functionality

Electronic Components and Systems

Scope

These are materials, process modules and integration technology for ***novel devices and circuits that enable advanced functionality*** *(sensing, actuating, energy harvesting and storage, connectivity, biomedical, etc), including (wafer or flexible)* ***substrate technologies****.*

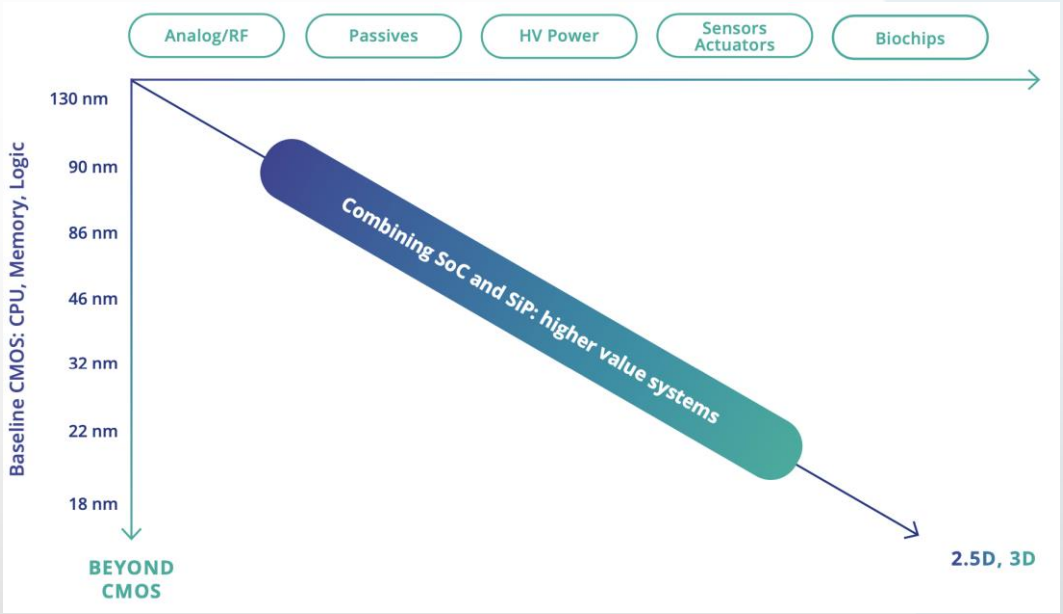
Integration *of the* ***logic/memory*** *building blocks* ***with the non-logic/non-memory*** *building blocks on a single chip* - ***power chips, sensors, NEMS/MEMS (microelectromechanical systems), energy harvesting and storage devices, RF chips, photonic functionalities.***

Expected achievement

Implementation of **pilot lines for integrated application-defined** sensors, novel IoT solutions, complex sensor systems and new (bio)medical devices, new RF and mm-wave device options (including radar), photonics options, electronics and packaging solutions.

Applications for **large-area, lightweight, robust and structurally integrated electronics.** **Boundaries** between µ-electronics, semiconductor electronics, photonics and flexible (stretchable) electronics **will slowly disappear**.

Strategic collaborative EU projects for European industry to become more independent, development of a EU-based supply chain.



Connect the application needs and system-level innovation to the technology innovation.

Major challenge 2: Novel devices and circuits that enable advanced functionality

E C S
Electronic Components and Systems

Scope

*These are materials, process modules and integration technology for **novel devices and circuits that enable advanced functionality** (sensing, actuating, energy harvesting and storage, connectivity, biomedical, etc), including (wafer or flexible) **substrate technologies**.*

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PRIORITY

Application-specific logic

Neuromorphic computing. Logic integration with power management devices, icompatibility with harsh environments.
Logic integration with RF, optical or sensor technologies.
Ultra-low power (ULP) technology platform and design.

PRIORITY

Advanced sensor technologies

Mechanical, chemical, physical sensors and biochemical sensors *(fluidics)*.
Transmitter/receiver and active phased array imaging.

PRIORITY

Advanced power electronics technologies

Si-based, BCD, SiC, GaN, Ga2O3, etc; larger diameter substrates for cost-sensitive power solutions.
Higher power density and frequency, wide-bandgap materials for high temperature electronics, CMOS/IGBT, integrated logic, uni- and bipolar, high voltage classes, lateral to vertical architectures.
Energy harvesting, storage, efficiency, autonomy

PRIORITY

Advanced RF and photonics communication technologies

more energy-efficient control of TX (5G, 6G preparations), new energy-efficient RF and mm-wave integrated device options (e.g. SiGe/BiCMOS, FD SOI, CMOS, PIC).
RF cryogenic electronics for QIP.
CMOS- (and packaging-) compatible MOEMS and micro-optics, nanophotonics, optical interconnections, photonics-enabled, and integrated light emitters.

PRIORITY

Electronics on flexible and structural substrates

Novel (semi)conducting, insulating and encapsulation materials for more reliable devices, and novel substrate materials, biodegradable materials

WS 5 "Multifunctional Integration"

Timeline

Novel devices and circuits that enable advanced functionality

MAJOR CHALLENGE	TOPIC	SHORT TERM (2021–2025)	MEDIUM TERM (2026–2029)	LONG TERM (2030–2035)
Major challenge 2: Novel devices and circuits that enable advanced functionality	**Topic 2.1:** Application-specific logic integration	• ULP 18 nm FDSOI technology integration	• 12 nm FDSOI technology integration • New architectures for neuromorphic computing • 3D stacking for monolithic integration	• 3D monolithic integration
	Topic 2.2: Advanced sensor technologies	• Continuous improvement of sensitivity (imagers, IMU, etc), range (lidar), and reduction of sensor area and energy consumption • Development of miniaturised low power chemical sensors • Development of biomedical sensors integrated with micro/nanofluidics • Heterogeneous integration of sensor technologies with (ULP) logic/memory technologies • 22 nm FDSOI for the IoT	• Quantum sensors • Ultra-low power chemical sensor systems for pollution monitoring • Energy autonomous sensor systems • Multi-sensor systems for IoT • Integrated biomedical sensor system • Heterogeneous integration of sensor technologies with novel device, circuit and systems memory and computing concepts • 12nm FD-SOI for IoT	• Nanoelectronic sensor devices with individual molecule sensitivity and selectivity • Nanoelectronic biomedical sensor systems • Monolithic integration of sensor technologies with novel devices, circuit and systems memory and computing concepts • Beyond 10 nm FDSOI for IoT
	Topic 2.3: Advanced power electronics technologies	• Silicon, BCD, SiC and GaN-based technologies and substrate materials • Energy-efficient systems, including energy harvesting	• New CMOS and IGBT processes • Smart GaN devices (combining logic and power devices) • Vertical GaN power devices • Towards 300 mm GaN and 200 mm SiC substrates • Energy-autonomous systems • Energy harvesting and energy storage systems	• B-Ga_2O_3 • Diamond
Major challenge 2: Novel devices and circuits that enable advanced functionality	**Topic 2.4:** Advanced RF and photonics communication technologies	• Enable 5G connectivity • RF and mm-wave integrated device options building on, for example, SiGe/BiCMOS (increase of ft), RF and FDSOI, CMOS, PIC • GaN/Si and GaN/SiC technologies • Next-generation RFSOI • 300 mm photonic SOI • 200 mm POI	• Enable 6G connectivity? • MOEMS and micro-optics, optical interconnections and light emitters • Photonic SOI next generation • Advanced RF filter materials and technologies	• RF cryogenic electronics for QIP
	Topic 2.5: Flexible and structural substrate electronics	• Increased reliability of materials and process techniques, reduction of pattern size • Development for displays, textiles and wearables (sensors) • Integration of conformable electronics on 3D surfaces	• Stretchable devices and displays • Flexible photonic components • Compostable electronics	• Seamless integration of µ-electronics, flexible electronic and photonics

Major challenge 3: Advanced heterogeneous integration and packaging solutions

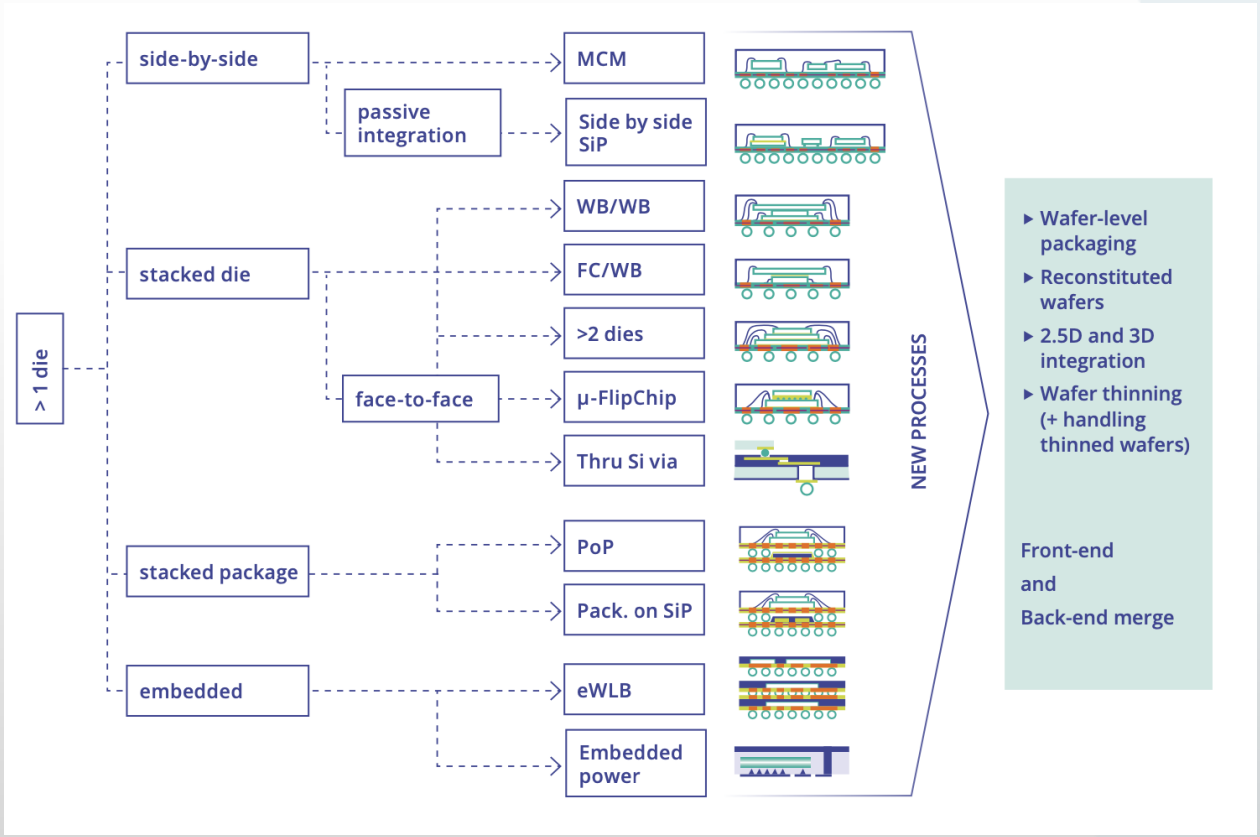
Electronic Components and Systems

Scope

- Advanced packaging and interconnection methods to bridge the scale gap between wafer dies of various technologies and printed circuit boards (PCBs)
- Advanced heterogeneous integration to include new functionalities in SiP

Goal

enable new solutions for the digital age and to ensure industrial competitiveness and European sovereignty



Major challenge 3: Advanced heterogeneous integration and packaging solutions

Electronic Components and Systems

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PRIORITY

Novel systems with advanced logic

(Heterogeneous / 3D) Integration with advance memory/logic circuits for Ultra-low power technology

PRIORITY

Advanced interconnect, encapsulation and packaging technologies

Vertical and horizontal integrations, TSVs;
Fan-out WLP;
Chip embedding;
Wafer-stacking;
Thermal management in packaging;

PRIORITY

3D integration technologies.

3D integration density improvement;
Chip-package-board co-design.

PRIORITY

Specific power and RF application technologies

RF Miniaturization for millimetre wave and THz applications;
Functional integration for package, e.g. antennas, passive components;
Packaging of wide-bandgap materials, SiC and GaN;
Cryogenic packaging for quantum tech.

PRIORITY

Enhanced reliability, robustness and sustainability technologies

Testing of separate components before integration;
Built-in self-test

WS 5 "Multifunctional Integration"

System of systems (SoS) & Internet of things (IoT)

Electronic Components and Systems

SoS/IoT are essential for digitization, a key point for the edge to cloud continuum, a hierarchical physical/digital infrastructure, providing the HW/SW elements to:

- map the physical world with the digital world,
- process data in various ways, where and when it is required,
- ensure a seamless flow of information, from the deep edge to the cloud.

Priorities span the entire SoS/IoT domain: materials, HW architectures, sensors, actuators, smart devices, processing, connectivity, interoperability, integration platforms, e2e trustworthiness, ...

T cover the phases of the ECS value chain
d to grow tenfold by 2025.

WS 4 AI, IoT, Advanced Control and Edge Computing

PRIORITY

Advanced computing, memory and in-memory computing concepts.

E.g. new materials, memory concept and technologies for mobile computing, and ultra-low power data processing at the IoT node level up to the highest possible performance.

PRIORITY

Novel devices and circuits that enable advanced functionality.

E.g. application-defined sensors, novel IoT solutions, complex sensor systems and new (bio)medical devices, new RF and mm-wave device options (including radar), photonics options, electronics and packaging solutions.

PRIORITY

Efficient physical/functional integration satisfying heterogeneous needs

IoT devices operate in heterogeneous environments, with different energy consumption and autonomy profiles, provides multiple types of information, heterogeneous functionalities, across sensing, actuation, connectivity, information processing, …

PRIORITY WS1

SoS and IoT architectures, supported by appropriate design and architecting tools.

PRIORITY WS1

Open SoS/IoT integration and orchestration platforms.

PRIORITY WS1

Support composability , complexity, evolvability, heterogeneity and diversity in integration and orchestration process.

PRIORITY WS1

- **Integration platforms interoperability**
- **Autonomous interoperability**
- **Existing and emerging SoS/IoT interop.**

PRIORITY WS1

Ensuring end-2-end cyber-security, safety and privacy of SoS/IoT.

Major challenge 4: World-leading and sustainable semiconductor manufacturing equipment and technologies

Electronic Components and Systems

Scope

Semiconductor manufacturing equipment ***for the high volume production of sub-3 nm node logic and memory*** *according to PPAC roadmap requirements,* ***chips/chiplets*** *with single and/or multi-node layers,* ***advanced functionality*** *devices and* ***heterogeneous integration*** *technology options.*

Expected achievement

The goal of the European equipment and manufacturing industry for advanced semiconductor technologies is to **lead the world in miniaturisation and performance** by supplying new equipment and new materials..

Moreover, European semiconductor equipment and **manufacturing technologies** will be **innovation leaders** in terms of the use of AI, machine learning in the operation of semiconductor fabrication, and in taking care of limited datasets for model training in a high-mix environment. Solutions for current and future factories will allow **high-productivity manufacturing of variable volume, and the energy-efficient, sustainable, resource- saving volume production of semiconductors.**

PRIORITY

Wafer fabrication equipment

Advanced patterning equipment and mask manufacturing, patterning and tuning, defect inspection and repair, metrology and cleaning.
Advanced holistic lithography using DUV, EUV and next-generation lithography techniques, such as e-beam and mask-less lithography, directed self-assembly (DSA) and nano-imprinting.
Multi-dimensional metrology (MDM) and inspection.
Productivity-aware design (PAD) techniques.
Thin film processes including future solutions.
Wet and dry processing.
Advanced nanomaterials and metamaterials.
Production of III-V, SiC, etc. substrates at relevant size.

PRIORITY

Assembly equipment

3D integration and interconnect
Equipment optimised for both high-volume large batches and low volume small batches.
Die separation, attachment, thinning, handling and encapsulation. Multi-component assembly on flexible, stretchable substrates & roll-to-roll.

PRIORITY

Test equipment

In-line and off-line technologies for the testing, validation and verification (TV&V) of heterogeneous chips and SiP.
Characterisation equipment for quality control at multiple levels and different scales.

PRIORITY

Dedicated equipment and manufacturing technology

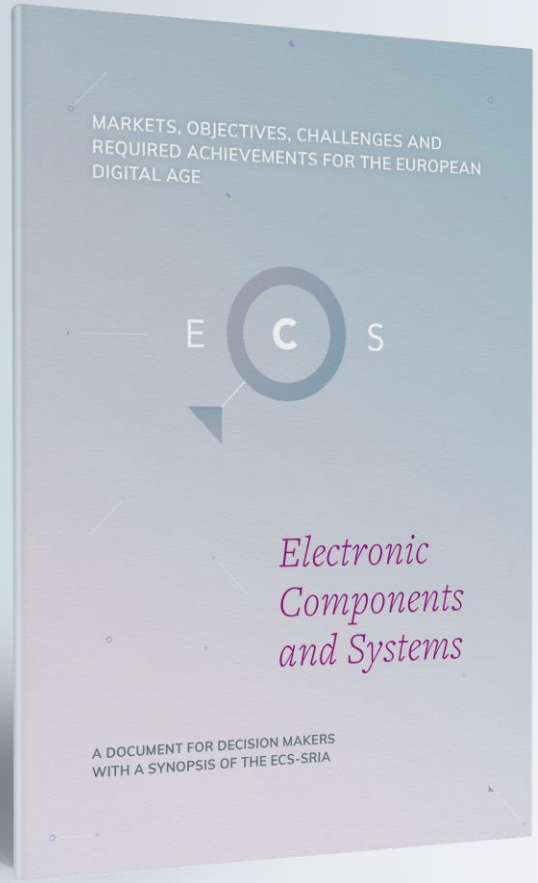
Dedicated equipment for manufacturing of electronics on flexible, structural and/or bio- compatible substrates.
Specific manufacturing technologies to enable flexible, sustainable, agile and competitive high-volume semiconductor manufacturing of high- quality, advanced functionality devices and heterogeneous integration technology options in Europe.
for the production and characterisation of advanced integrated photonics, as well as for the production of quantum computing chips.

Timeline

World-leading and sustainable semiconductor manufacturing equipment and technologies

Electronic Components and Systems

MAJOR CHALLENGE	TOPIC	SHORT TERM (2021–2025)	MEDIUM TERM (2026–2029)	LONG TERM (2030–2035)
Major challenge 4: World-leading and sustainable semiconductor manufacturing equipment and technologies	**Topic 4.1:** Wafer fabrication equipment for nanoscale patterning, layer deposition, metrology, and inspection for advanced logic and memory technologies	• Manufacturing equipment for 3 nm node logic and memory	• Manufacturing equipment for 1 nm node logic and memory • Equipment to enable novel switches, transistors and alternatives based on, for example, 2D materials, topologic insulator and spin-wave devices	• Manufacturing equipment for sub-1 nm node logic and memory
	Topic 4.2: Wafer fabrication equipment for new transistor front end of line (FEOL) and new interconnect back end of line (BEOL) concepts	• Manufacturing equipment for 3 nm node transistor and 3D heterogeneous integration interconnect concepts	• Manufacturing equipment for 1 nm node transistor and 3D monolithic integrated and optical interconnect concepts	• Manufacturing equipment for sub 1 nm node transistor and 3D monolithic and optical interconnect concepts
	Topic 4.3: Wafer fabrication equipment for new materials and processes	• Manufacturing equipment for 3 nm node materials and processes • Equipment for manufacturing of components with advanced nanomaterials • Production tools for III-V, GaN, SiC or other exotic material substrates	• Manufacturing equipment for 1 nm node materials and processes • Equipment for materials and processes for new eNVM types such as (high-density) ReRAM • Production tools for 300mm wafer substrates based on selected exotic materials	• Manufacturing equipment for sub 1 nm node materials and processes
	Topic 4.4: Assembly and test equipment enabling advanced packaging of single and/or multi-node chips/chiplets	• Assembly and test equipment for chip-to-wafer stacking, fan-out WLP, multi-die packaging, “2.5D” interposers and TSVs • 300 mm photonic SOI • 200 mm POI	• Assembly and test equipment to enable next-generation autonomous sensors, power electronics and RF/optical communication packaged ICs	



Thank you

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