

RISC-V - Create #1 Core Supplier incl. SW Toolchain & SW Eco-System

Perspectives for EU KDT

NXP Semiconductors, CTO Innovation Management & Tech Roadmaps
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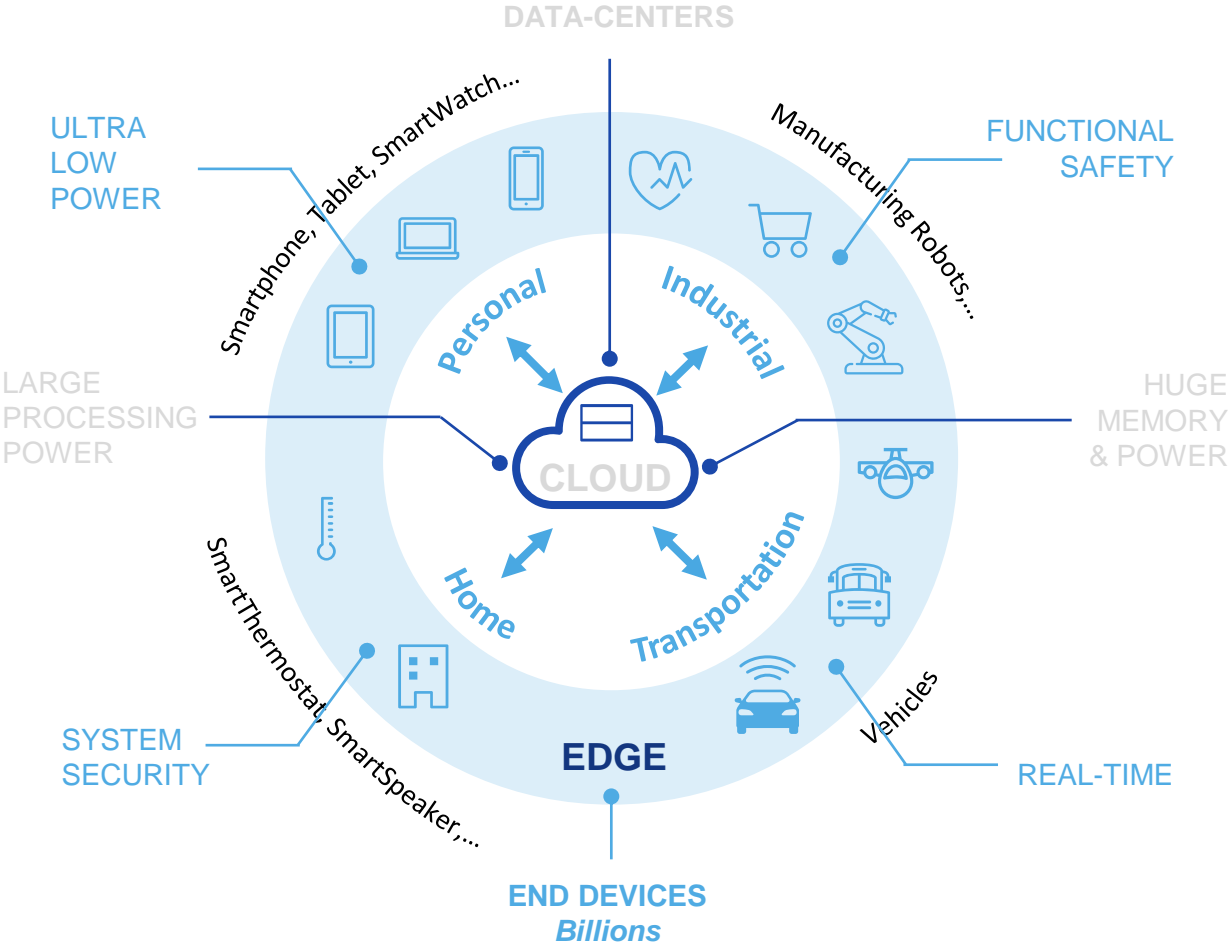
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RISE OF SECURE EDGE PROCESSING

EXPLOSION OF SMART DEVICES



**DATA COLLECTION, PROCESSING AND DECISIONS TAKEN AT THE EDGE,
EDGE DEVICES SECURELY CONNECTED TO THE CLOUD**



CORE LANDSCAPE – TODAY AND RISC-V TREND FOR COMING YEARS

Availability of General Purpose Processors

		Arm	RISC-V	
HW	SW	<ul style="list-style-type: none"> Established base 	<ul style="list-style-type: none"> Emerging options > 3yrs 	High Performance
		<ul style="list-style-type: none"> Mature Linux ecosystem 	<ul style="list-style-type: none"> Expect emerging open source ecosystem 	
HW	SW	<ul style="list-style-type: none"> Established base 	<ul style="list-style-type: none"> Open Source and commercial vendors Time to market 	Medium and Low Performance
		<ul style="list-style-type: none"> Mature ecosystem 	<ul style="list-style-type: none"> Growing open source ecosystem 	

Ability to enhance Instruction Set Architecture and modify GPP

		Arm	RISC-V
HW			<ul style="list-style-type: none"> Emerging vendors
SW			<ul style="list-style-type: none"> Vendor supplied tools

Availability of Accelerators

		3rd Party	RISC-V
HW		<ul style="list-style-type: none"> Scattered landscape 	<ul style="list-style-type: none"> Emerging vendors
SW		<ul style="list-style-type: none"> Scattered landscape 	<ul style="list-style-type: none"> Vendor supported SW ecosystem

RISC-V CORES & SW INVESTMENT

- General Purpose Cores GPP

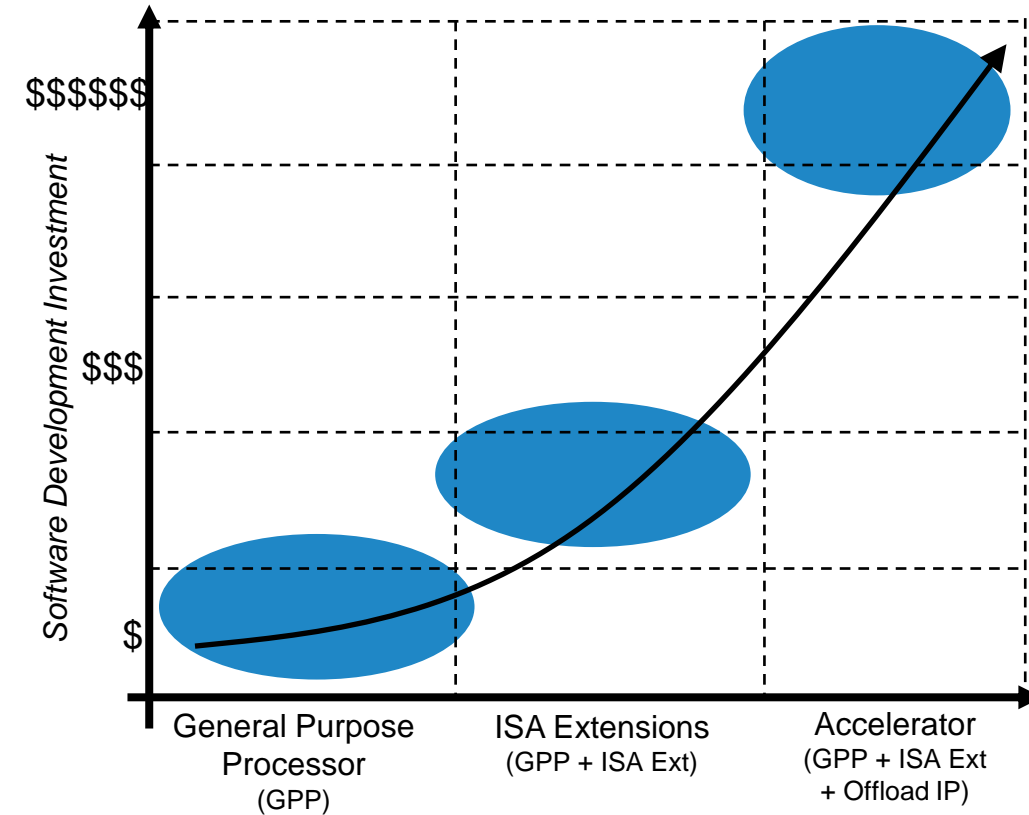
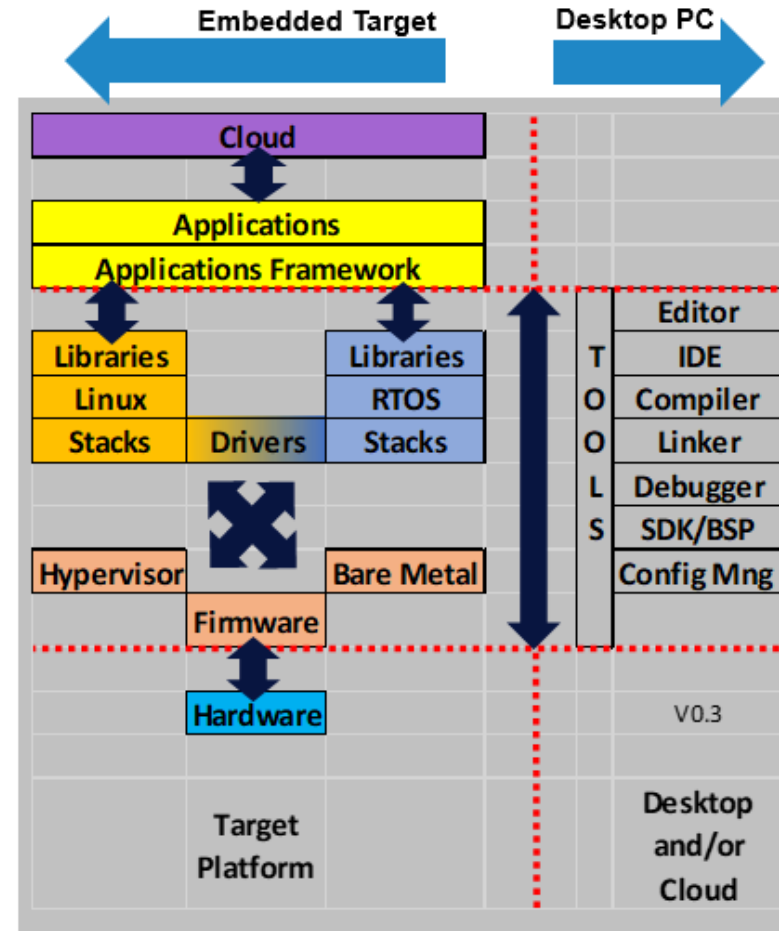
- Customer programmable cores used to execute the target software
- Leverage industry standard ISAs giving the widest access to open source and 3rd party target/tools SW

- ISA Extensions GPP + Instruction Extensions

- Customer programmable and/or hidden SoC cores with additional instruction extensions aimed at accelerating specific SW algorithms
- Vendor specific requiring proprietary SW target/tools development/SoC lifetime support

- Accelerators GPP + ISA-Ext + Offload HW IP

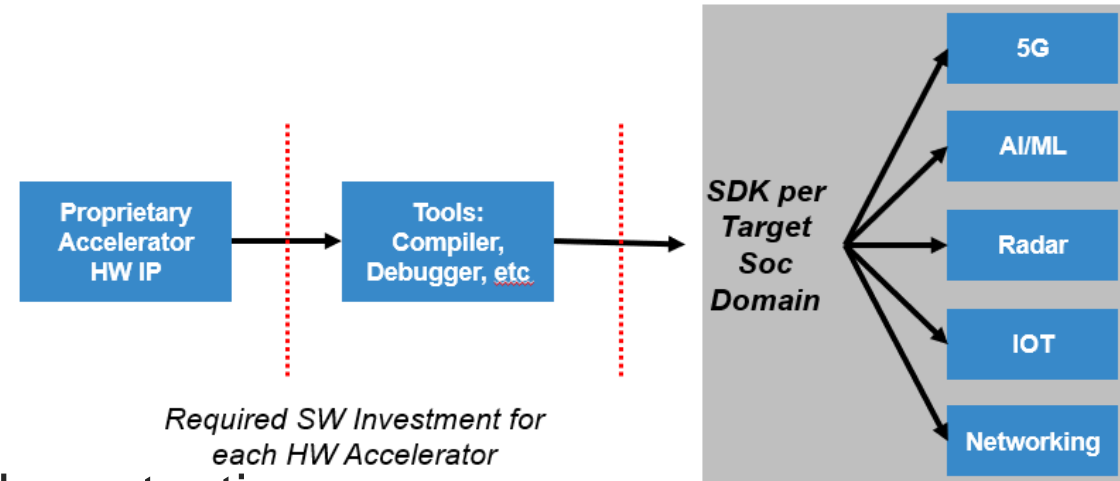
- Hidden SoC cores with both ISA-Ext and custom offload HW IP to accelerate SW algorithms
- Vendor specific proprietary system architectures requiring SW target/tools development/lifetime SoC support



GOAL HAS TO BE #1 CORE SUPPLIER INCLUDING SW TOOLCHAIN AND SW ECOSYSTEM

Software.

- The success of a core is determined by the SW ecosystem enabling its use
- Toolchain matching market requirements (e.g. automotive = Safety tool integrity)
- Software = The customer investment which needs protecting



... and yes, we need cores.

Robust. Proven. Lifetime support.

With the right performance for the use case.

No scattered and slow niche plays.



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