RISC V
in the ECSEL Programme

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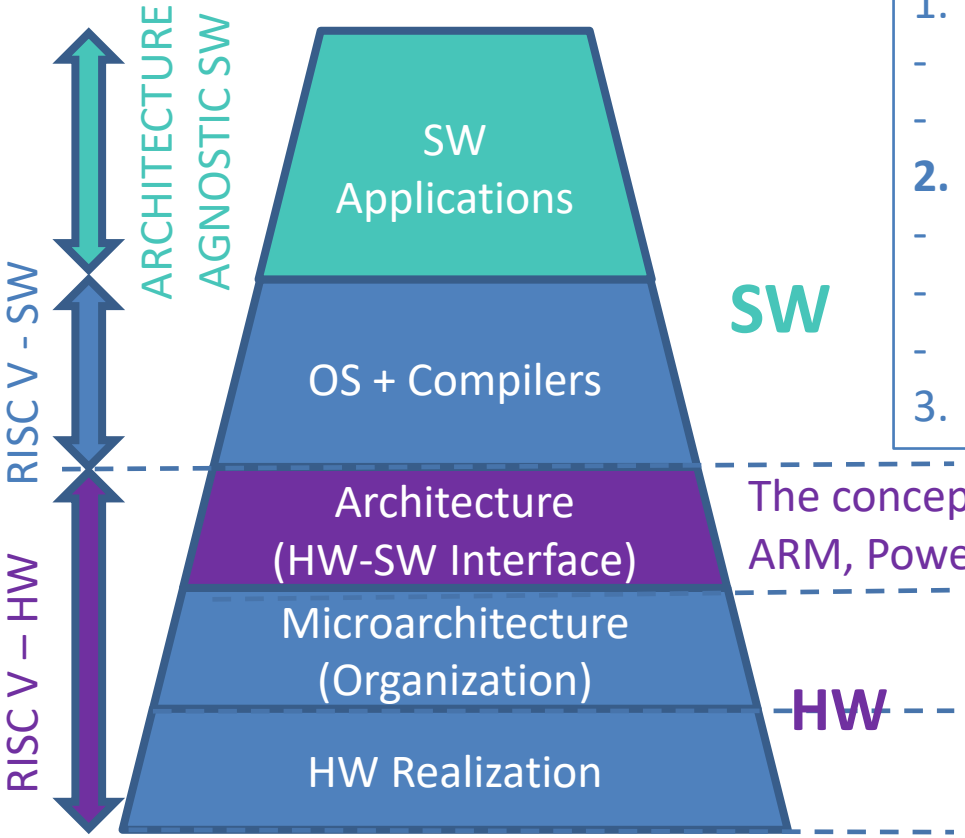
General Considerations

Hierarchy of the General Computer Design



In **ECSEL projects**:

1. Computer Architectures are:
- **NOT a core objective**; BUT!
- addressed in many **projects' tasks** as development platforms.

2. **RISC V** is the main open source HW architecture. Activities concern:
- Architecture Extensions (e.g., accelerators, co-processors)
- (Low Power/High Performance) microarchitectures (e.g., implementations)
- (Low Power) HW realizations (e.g., FDSOI)

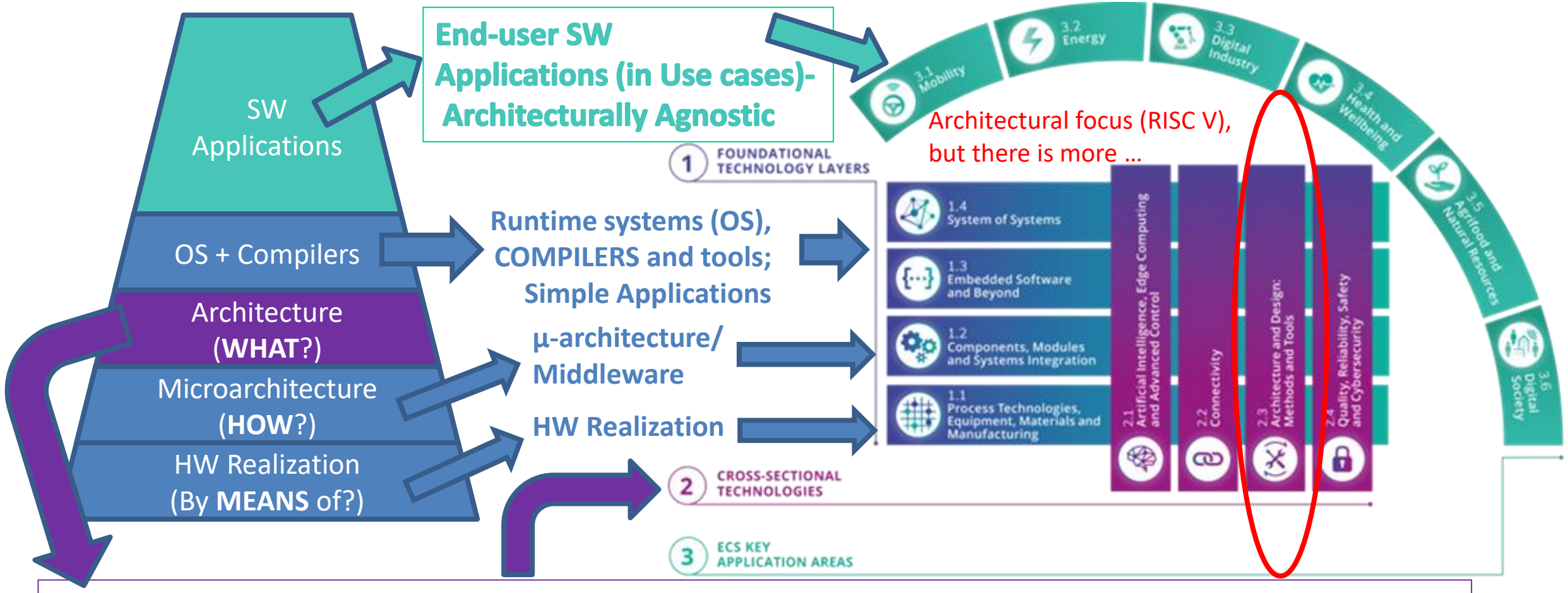
3. SW support for RISC V: tools for design, verification, testing, etc.

The conceptual structure and functional behavior as seen by the Programmer (RISC V, ARM, Power PC, etc.) – abstracts **complexity** and allows **independent** SW/HW design.

The logical organization of the dataflows and controls of a computer system (e.g. bus widths, gates, flip-flops, caches, timing, etc.)

The physical structure embodying the implementation (e.g. FD-SOI)

Architectures in the ECS-SRIA



ARCHITECTURES + Tool chains + the entire SW stack (middleware, system SW, Apps)

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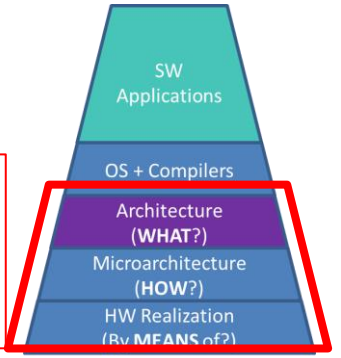
RISC V Activities per Project (1/7)

OCEAN 12 (2017-1-IA) - Opportunity to Carry European Autonomous driviNg further with FDSOI technology up to 12nm node –

RISC V in the project:

- **Architecture (functionality):** An ultra-low power RISC-V microcontroller with **signal processing capabilities** will be implemented.
- **Microarchitecture (organization):** A 12FDX ultra-low power RISC-V Micro-Controller Unit (MCU) based research platform will be developed. This MCU platform targets modelling, estimation and **optimization of power and timing** for embedded systems.
- **Realization (Main Focus!) :** OCEAN12 will develop new processors and applications design that leverage Fully Depleted Silicon On Insulator (**FD-SOI**) technology to offer the industry's **lowest power consuming processor**, especially for **automotive and aeronautic applications**.



HW DESIGN COVERAGE:
All 3 layers, ARCHITECTURE (WHAT), MICROARCHITECTURE (HOW), REALIZATION (BY MEANS OF);
System SW and Tools: WEAKLY COVERED.

RISC V Activities per Project (2/7)

CPS4EU (2018-1-IA) - Cyber Physical Systems for Europe - This project is **architecturally agnostic,** but considers **RISC V** as an important reference architecture.

RISC V in the project:

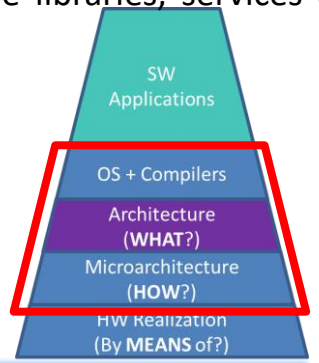
As part of this project, the involved partners will develop computing **architectures** (including **RISC V**) optimized for several CPS use cases (i.e., optimized **microarchitectures**). The project will:

1. Develop 4 key enabling technologies (computing, connectivity, sensing, cooperative systems) - i.e., **Architectures** (**what?**) and **microarchitectures** (**How**?);
2. Incorporate these CPS modules through **pre-integrated architectures (including RISC V)** (i.e., develop **microarchitectures**) and design **tools**;
3. Instantiate these **architectures** in dedicated use cases from **strategic application**: automotive, smart grid and industry automation;
4. Improve CPS awareness and usage for all industrial sectors.

For each identified architecture (including **RISC V**):

- the required hardware components will be integrated: **Microprocessors** (ARM cores, MPPA, **RISC V**, etc.), **Coprocessors** such as TPUs (Tensor processing unit), etc., Security **IPs** (Root of Trust, Cryptographic accelerators, etc.), Security **features** (Secure Boot, Secure DDR, TPM, etc.), **Communication** links (deterministic interconnect, LTE, Ethernet, IoT protocols, PCIe, sensors, etc.). (i.e., develop **microarchitectures**)
- the required **software components** will be integrated: Operating system, Drivers, Heterogeneous middleware, Software libraries, services and components. (i.e., **system SW**)
- Validation and test environment will be built to evaluate the architecture. (**tools**)

HW DESIGN COVERED: ARCHITECTURE (WHAT), MICROARCHITECTURE (HOW);
HW DESIGN NOT COVERED: REALIZATION (BY MEANS OF);
System SW and Tools: COVERED (MAIN FOCUS).



RISC V Activities per Project (3/7)

VALU3S (2019-2-RIA) Verification and Validation of Automated Systems' Safety and Security

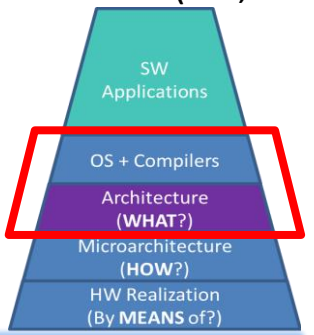
VALU3S aims to design, implement and evaluate state-of-the-art **V&V methods and tools** in order to reduce the time and cost needed to verify and validate automated systems with respect to safety, cybersecurity and privacy (SCP) requirements. Wide application coverage: 13 use cases with specific SCP requirements from 6 domains of automotive, industrial robotics, agriculture, Aerospace, railway and health.

RISC V in the project:

The core activities in this project are **architecturally agnostic**, but **RISC V** is considered as a replacement of a traditional ARM architecture:

- In a proven-in-use system a challenge is to replace core parts without losing functional safety, e.g., replacing an ARM CPU with a RISC-V CPU. (i.e., new **Architecture**)
- RISC-V CPU test suite for motion control systems. The test suite developed during VALU3S will add to the current V&V. (i.e., **Tools**)
- VALUE3S results will help to increase today's test coverage and reduce related efforts especially for RISC-V based future industrial drive controllers. (i.e., **Tools**)
- will refine the common system level requirements of their use case and derive additional test cases for the new RISC-V CPU (i.e., **Tools**)

HW DESIGN COVERED: ARCHITECTURE (WHAT);
HW DESIGN NOT COVERED: MICROARCHITECTURE (HOW), REALIZATION (BY MEANS OF);
System SW and Tools: COVERED.



RISC V Activities per Project (4/7)

FRACTAL (2019-2-SP2) A Cognitive Fractal and Secure EDGE based on a unique Open-Safe-Reliable-Low Power Hardware Platform Node

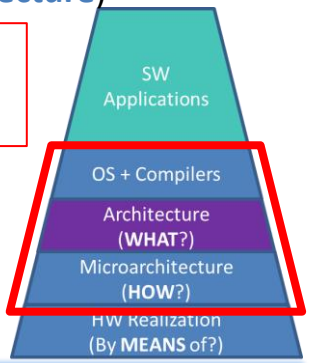
The objective is to **create a reliable computing node** that will create a **Cognitive Edge** under industry standards. This computing node will be the building block of scalable Internet of Things (from Low Computing to High Computing Edge Nodes).

RISC V in the project:

- A **single chip** solution based on RISC-V: a multicore platform with 64-bit RISC-V cores and a multi-level memory hierarchy including safety features, Safety aware RISC-V multicore, We can foresee a new family of RISC-V cores with enhancements (i.e., **architecture** and **microarchitecture**).
- **Cognitive edge nodes** will be presented in two flavors (50%-50%) : (1) a partially constrained commercial node on the **Xilinx VERSAL (ARM)** platform and (2) a **fully flexible customizable** node with **RISC-V** cores and accelerators based on the open-source PULP (parallel ultra-low power) platform. (i.e., **architecture** and **microarchitecture**)
- Appropriate **hypervisors** or **comparable software** layers and **drivers** will be integrated into Linux Kernels on the RISC-V nodes, with the aim of providing a software layer that supports holistically the management of safety, security, low-power operation, and cognitive awareness. (i.e., **System SW**)
- **AI** integration techniques in **RISC-V** devices will be spread in other sector of activities (Automation, Autonomous Vehicle, IoT, Industry 4.0, Biomedical sector). (i.e., **architecture** – **WHAT**?)
- The **integration of multiple heterogeneous hardware components** in the RISC-V platform may be challenging (i.e. **microarchitecture**)

!!! Partners in FRACTAL that are **members of the RISC-V foundation** will be **active in the working groups of RISC-V** to influence the adoption of improvements of RISC-V ISA as a result of the work in FRACTAL.

HW DESIGN COVERED: ARCHITECTURE (WHAT), MICROARCHITECTURE (HOW);
HW DESIGN NOT COVERED: REALIZATION (BY MEANS OF);
System SW and Tools: COVERED.



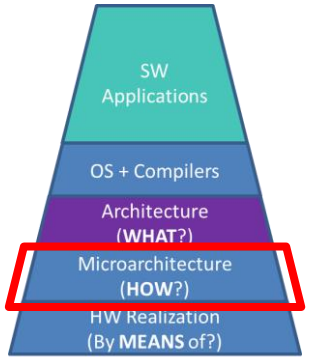
RISC V Activities per Project (5/7)

Energy ECS (2020-1-IA) Smart and secure energy solutions for future mobility

The project focuses on the **interface of energy and mobility** as well as **related ICT and electronics**. The project concept builds on six use cases that represent different angles of future mobility and energy. The R&D will also apply artificial intelligence, machine learning, immersive technologies, IoT, ultra-low power technologies, advanced algorithms and software. All technologies will be designed for cyber-security and reliability.

RISC V in the project:

One project activity will supply the memory IP that is optimized for the **low power platform**, targeting a machine learning application. The system will accommodate a programmable **RISC-V processor that organizes multiple hardware accelerators**, as well as a significant number of **memories** for 1) the processor's **instructions and data**, and 2) **data storage for processing and accelerators**. (i.e., **microarchitecture – HOW?**)



HW DESIGN COVERED: MICROARCHITECTURE (HOW);
HW DESIGN NOT COVERED:ARCHITECTURE (WHAT), REALIZATION (BY MEANS OF);
System SW and Tools: NOT COVERED.

RISC V Activities per Project (6/7)

StorAIge (2020-1-IA) Embedded storage elements on next MCU generation ready for AI on the edge

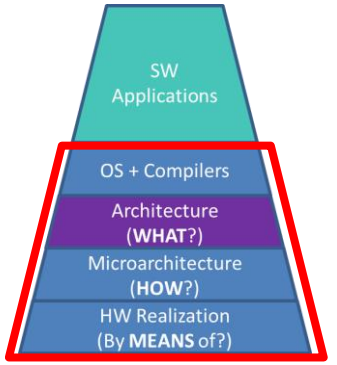
The main objective of the storAIge project is the development and industrialization of **FDSOI 28nm** (i.e., **realization**) and next generation embedded Phase Change Memory (**ePCM**) world-class semiconductor technologies enabling competitive Artificial Intelligence (**AI**) for Edge applications. The project is targeting chipset and solutions with very efficient memories and high computing power targeting **10 Tops per Watt** (i.e., **microarchitecture**).

The next generation of FDSOI ePCM will be main path for general purpose advanced microcontrollers usable for large volume Edge AI application with the best compromise on three requirements: **performances**, **low power** and adequate **security**.

On top of the development and industrialization of silicon process lines and SoC design, storAIge will also address new design methodologies and **tools**.

RISC V in the project:

The core activities in this project are **architecturally agnostic**, but it considers **libraries of IP** components around the standard **RISC-V**-based ecosystem, and AI-based **accelerators** (i.e., **architecture** and **microarchitecture**).



HW DESIGN COVERAGE:
All 3 layers, ARCHITECTURE (WHAT), MICROARCHITECTURE (HOW), REALIZATION (BY MEANS OF);
System SW and Tools: Tools COVERED.

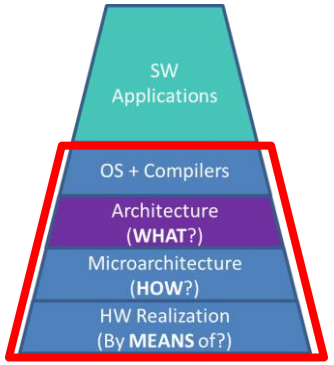
RISC V Activities per Project (7/7)

DAIS (2020-2-RIA) Distributed Artificial Intelligent Systems

The project will research and deliver distributed artificial intelligent systems. It will not research new algorithms, as such, but solves the problems of running existing algorithms on vastly distributed **edge devices**. The research and innovation activities are organized around eight complementary and mutually supportive supply chains.

RISC V in the project:

The project will develop a **new edge hardware** for near-sensor data processing as well as a **secure RISC-V processor** (i.e., **architecture**) for the edge. This will provide the edge with **low-power, low latency, and highly secure hardware** (i.e., **microarchitecture**) platform based on **open source RISC-V** processors with **AI accelerators** (i.e., **architecture** and **microarchitecture**). **Power efficiency** will be achieved by **combining digital and analogue RRAM**-based approaches (i.e., **realization**) as well as in **software** by fine and course-grained **reconfiguration** to achieve power-efficient acceleration over several algorithm classes.



HW DESIGN COVERAGE:
All 3 layers, ARCHITECTURE (WHAT), MICROARCHITECTURE (HOW), REALIZATION (BY MEANS OF);
System SW and Tools: System SW COVERED.

Conclusions

- In ECSEL projects, open source processor architectures are mainly represented by **RISC-V activities within tasks**
- The ECSEL portfolio covers a variety of RISC V aspects at a project task level, including:
  - **Architecture** Extensions (e.g., accelerators, co-processors – WHAT?);
  - (Low Power/High Performance) **microarchitectures** (e.g., implementations – HOW?);
  - (Low Power) HW **realizations** (e.g., FDSOI – By MEANS of?);
  - **SW support** for RISC V: System SW and tools for design, verification, testing, etc.
- **Compilers**, **System software** and **Development tools** are important for architecture's success (ref. - ARM).
- Mind that ARM was also an open source hardware once …
- RISC V has a potential to become a **de-facto standard** for open source HW.
- Several European entities and ECSEL participants are part of the **RISC V initiative bodies** – the more the better…
- Europe is **missing own core architecture (except ARM?)** established in industry and on the market - keep an eye on the USA, but do not overlook Asia.
- Many potentially interesting **unexplored areas** – e.g., **certification**, **benchmarking**, **scalability** of architectures, **cooperation** with other initiatives (EuroHPC).