Pilot lines in the Chips Act

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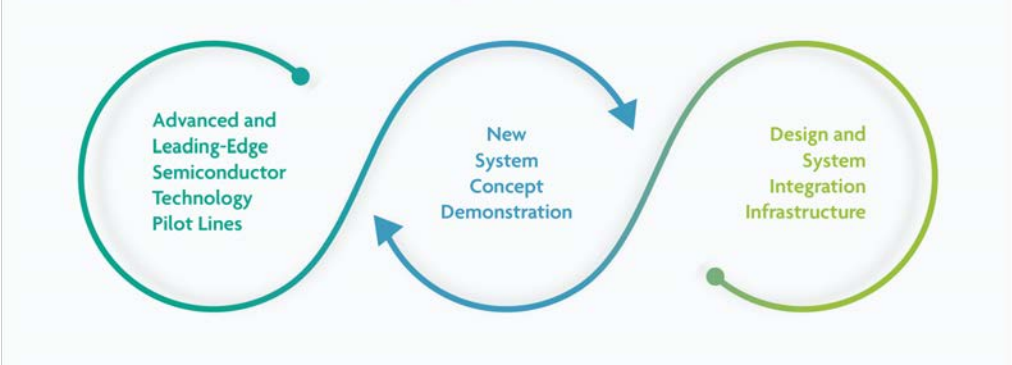
General aspects of the Chips for Europe Pilot lines

European technology and innovation leadership

The goal of the Chips for Europe Initiative is to support large-scale technological capacity building and innovation throughout the Union to enable the development and deployment of cutting-edge and next generation semiconductor and quantum technologies that will reinforce the Union's advanced design, systems integration, chips production capabilities and skills, including emphasis on start-ups and scale-ups.



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Pilot lines key outcomes

Key outcomes

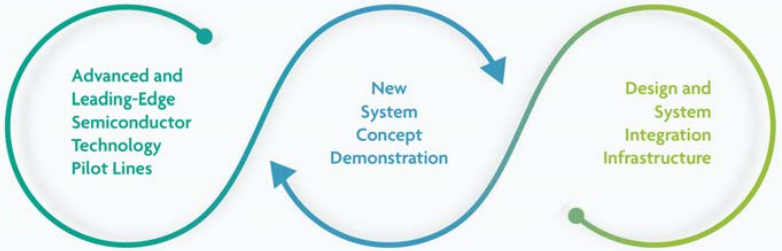
Sustain a **product and service innovation pipeline** at the level of tools, products and services, supported by European manufacturing in advanced and leading-edge semiconductor technology.

Infrastructure for **innovative and disruptive idea validation** on all aspects of the value chain (materials, equipment, manufacturing, device, circuit, key functional systems).

IP, knowledge transfer to European industry, scale-ups and start-ups. Allowing for **early prototyping and demonstration** and building the value chain to production.

Building a strong **European workforce**, through concerted actions through all segments of education, including programmes for retraining professionals.

Making Europe an **attraction pole for talent, innovation and investors**, leading to a grown or regained position in all aspects of the semiconductor value chain.



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European RTO alliance

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Pan-**European** alliance
For **European Technology and Innovation Leadership**

Research Fab Microelectronics Germany (FMD)

Facts & Figures

11 institutes from **Fraunhofer**

2 institutes from **Leibniz**

Approx. **4,500** employees with **2,635** scientists

560 m EUR Budget

200 m EUR projects/industry

235 m EUR projects/public funding

125 m EUR basic funding

19.500 m² cleanroom space with **ISO9001 Certification;**
1 MES over 10 institutes

2.200 tools/equipment in **13 cleanrooms**

2.2 bn EUR assets / investment

Design (down to 10/12 nm)
Wafer Processing:
GaAs/InP (4"), SiC (6")
Si, SiGe, GaN (8"), Si (12")
Advanced Packaging up to 12"; 600 mm panel
System Integration
Test & Characterization

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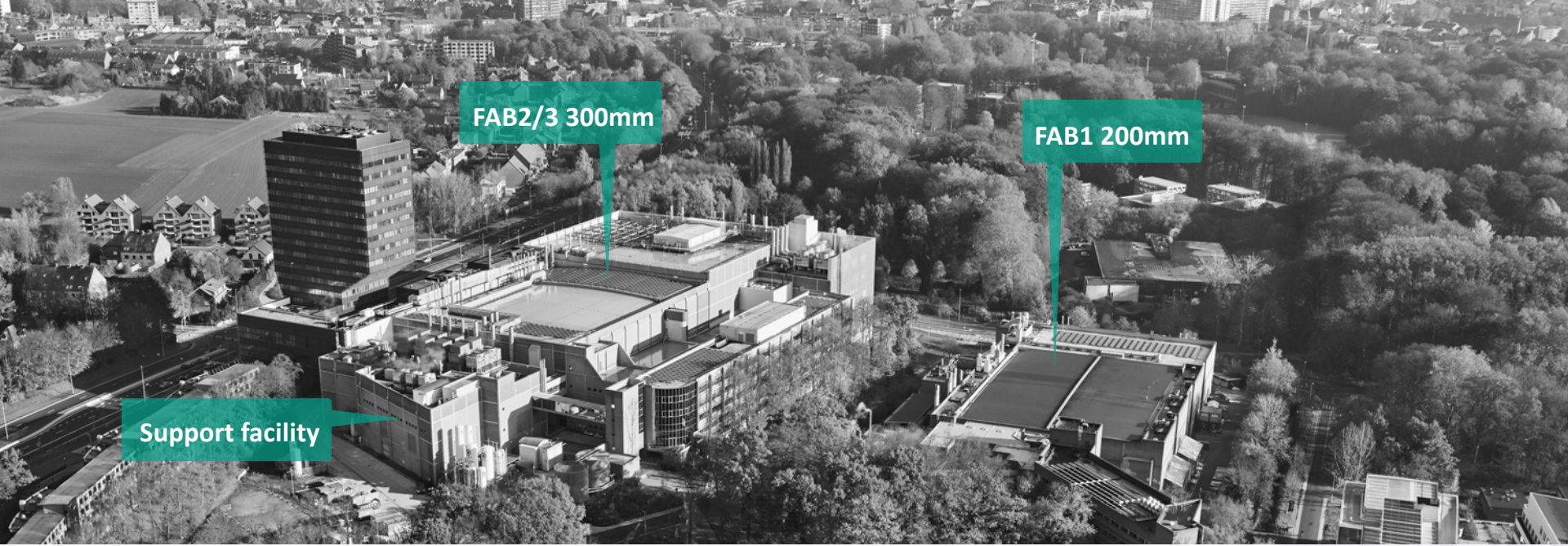
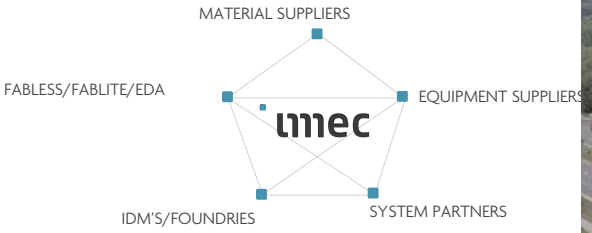


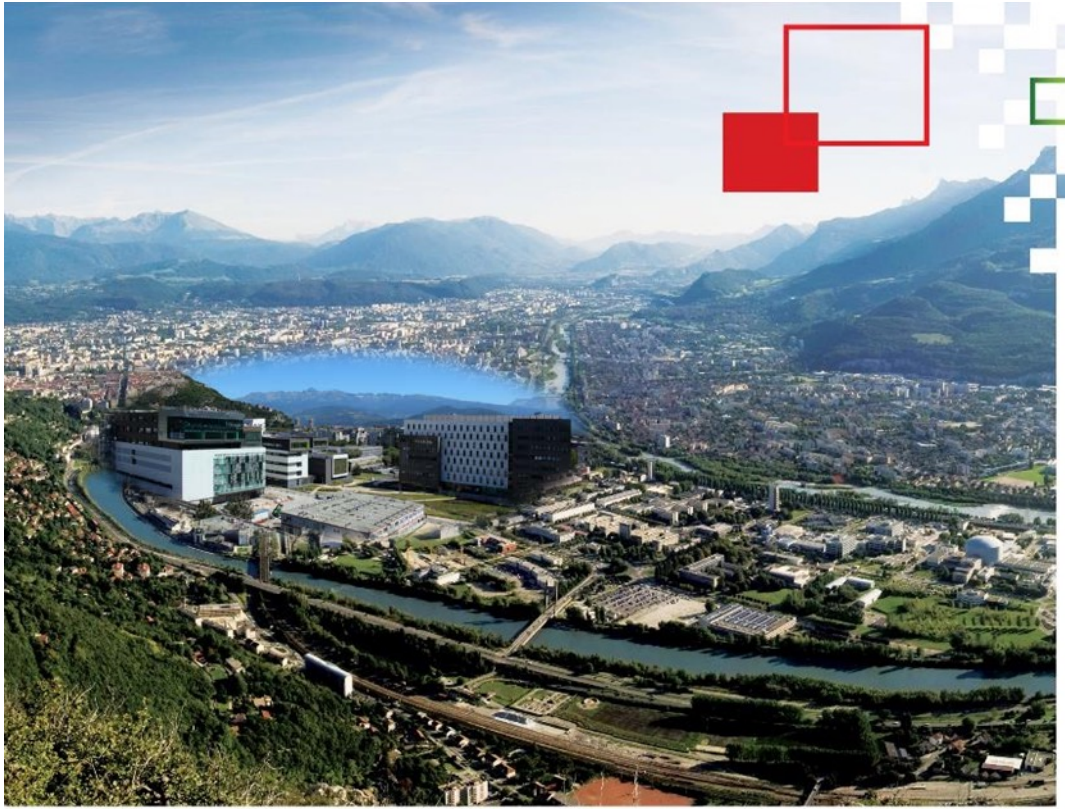
WORLD-CLASS INFRASTRUCTURE
> 12,000 M² CLEANROOM
CAPACITY

MORE THAN
5,000 SKILLED PEOPLE
FROM OVER 95 NATIONALITIES

Networked innovation model



CEA-LETI



LETI AT A GLANCE

- Founded in **1967**
- France, USA, Japan
- **2,000** People
- **> 2,760** Patents in Portfolio
- **350** Industrial Partners
- **> 65** Startups Created
- **10,000 m²** Cleanroom 200-300mm
- **315 M€** Budget
  85% from R&D contracts

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Pan European Pilot Line Facility – Categorizing pilot lines

Definition: RTO Pilot Lines and Industrial Pilot Lines

RTOs Pilot Lines „Innovation Push“		Industrial Pilot Lines „Scale Up“
Exploratory Services (lower TRLs)	Small Scale Production (mid to high TRLs)	First Industrial Deployment (highest TRLs)
Delivery of Prototypes ▪ Basic architectures and feasibilities for products at an early stage (e.g. for proof-of-concept) ▪ Processes are far from final maturity ▪ PDK* drafted, initial models in place	**Delivery of small volume** ▪ Technology and Processes can already be used for prototypes and products ▪ Technology frozen, customer specific adaptations possible ▪ PDK* available ▪ Small scale production capacity available (industrial grade)	**First delivery of qualified Products** ▪ Technology, Processes and Production Methodology under evaluation ▪ Up-scaling of a R&D project ▪ Yield still to be improved, thus, no competitive production possible yet ▪ PDK* finalized

RTOs
Research

Industry
Production

* **PDK**: process design kit, model of the fabrication process to be used for the **chip design**

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A balanced and phased approach for innovation in mature and leading edge semiconductor technology.

- **Heterogeneous integration, packaging** — Chiplet ecosystem / multi-functionality
- **Power, MEMS, specialties …** — Application specific components & subsystems
- **FDSOI generations** — FDSOI 22nm → 10nm → 5nm GAA
- **Planar transistors base** — 28/22nm
- **FinFET base** — 16nm... ...12nm → 10nm → 5nm

Expansion of EU advanced production facilities and growth of production of derivatives based on increased demand via use of pilot lines and design centers

- European IP build up on **nanosheet base – Gate All Around** (manufacturing capacity justified by increased demand)

Production of nanosheet generations - '2nm'

- Pathfinding, demonstration at pitch and system concept demonstration **in Pilot line facility**
  - FDSOI track → 10nm
  - Research PDKs projecting logic nodes 2nm (2024) to 7Å node (~2030): Enables existing IP look-ahead benchmarking / Understand the impact of future inflections like Forksheets, back-side power distribution, CFETs and 2D material channels on product roadmaps
  - 3D heterogeneous integration an Chiplet implementation
  - Accelerate the early-stage pilot lines Quantum, Neuromorphic exploration, Analog and Mixed signal / Power / Si Photonics
  - Secure chips
  - Sustainability

Pilot line infrastructure supported by extended network of connected design centers

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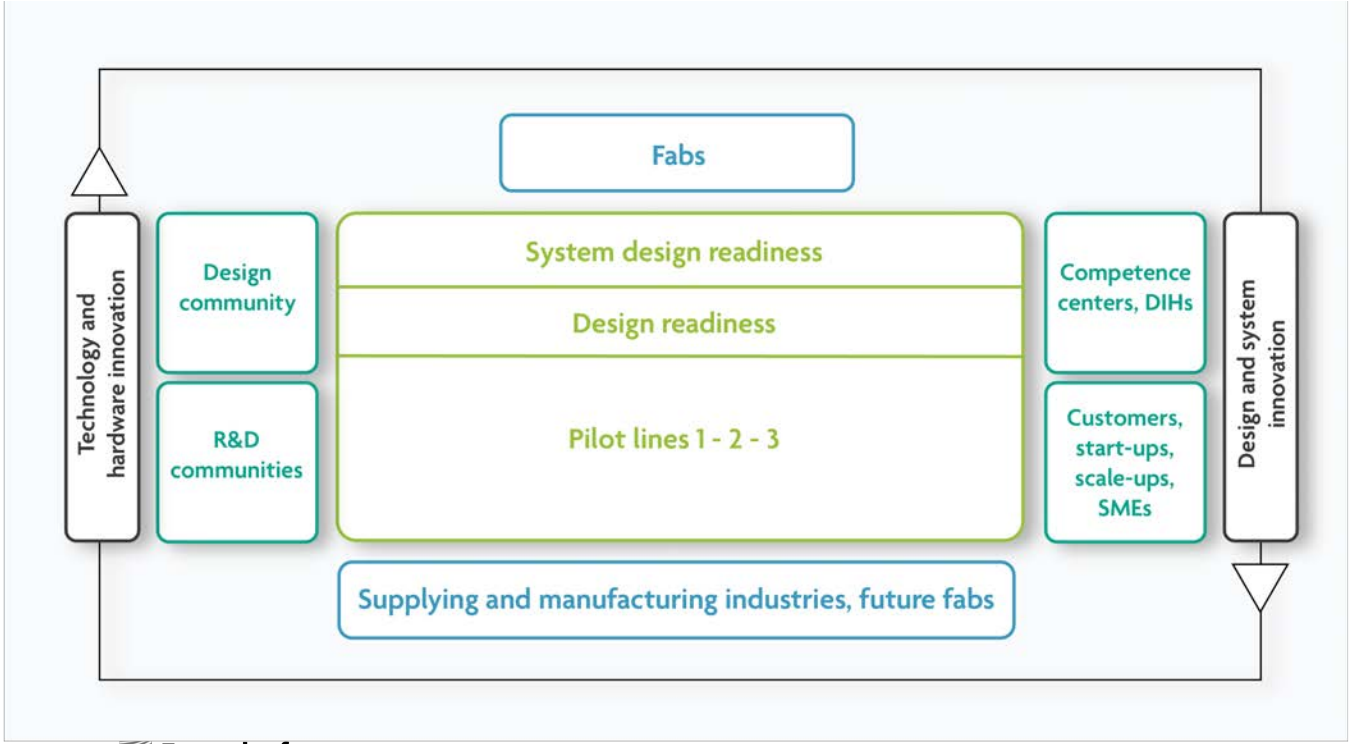
European Pilot Line innovation network



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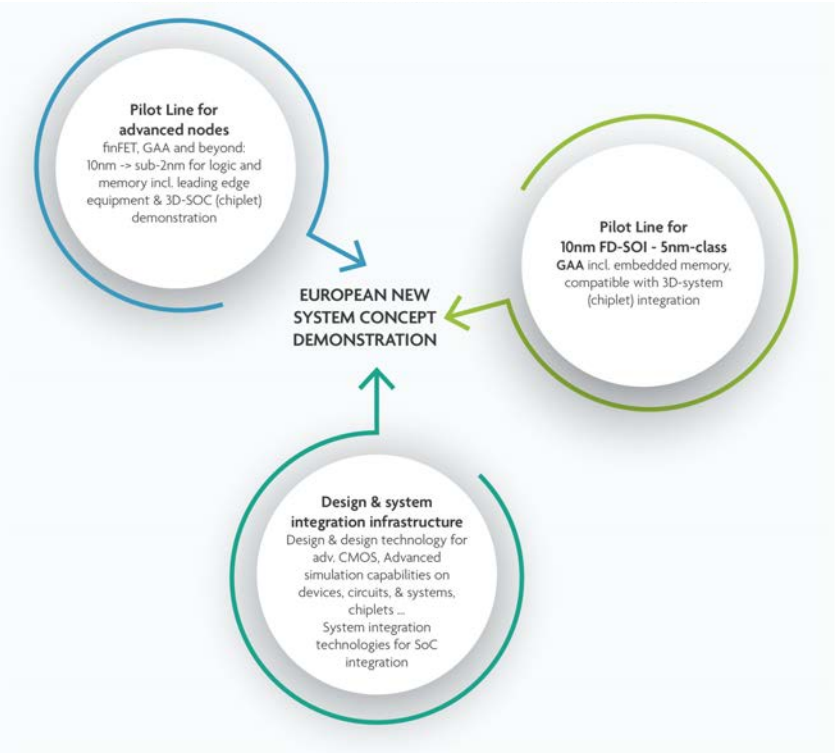
Profiling the contribution from the leading RTOs



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Deliver all process technology modules for most advanced IC nodes

Develop and demonstrate future equipment & materials solutions

Provide platform for concept demonstration & prototyping of future HPC & digital system innovation

SECURE European IP and technology

ENSURE European leadership on equipment & materials

CREATE the market and demand in Europe

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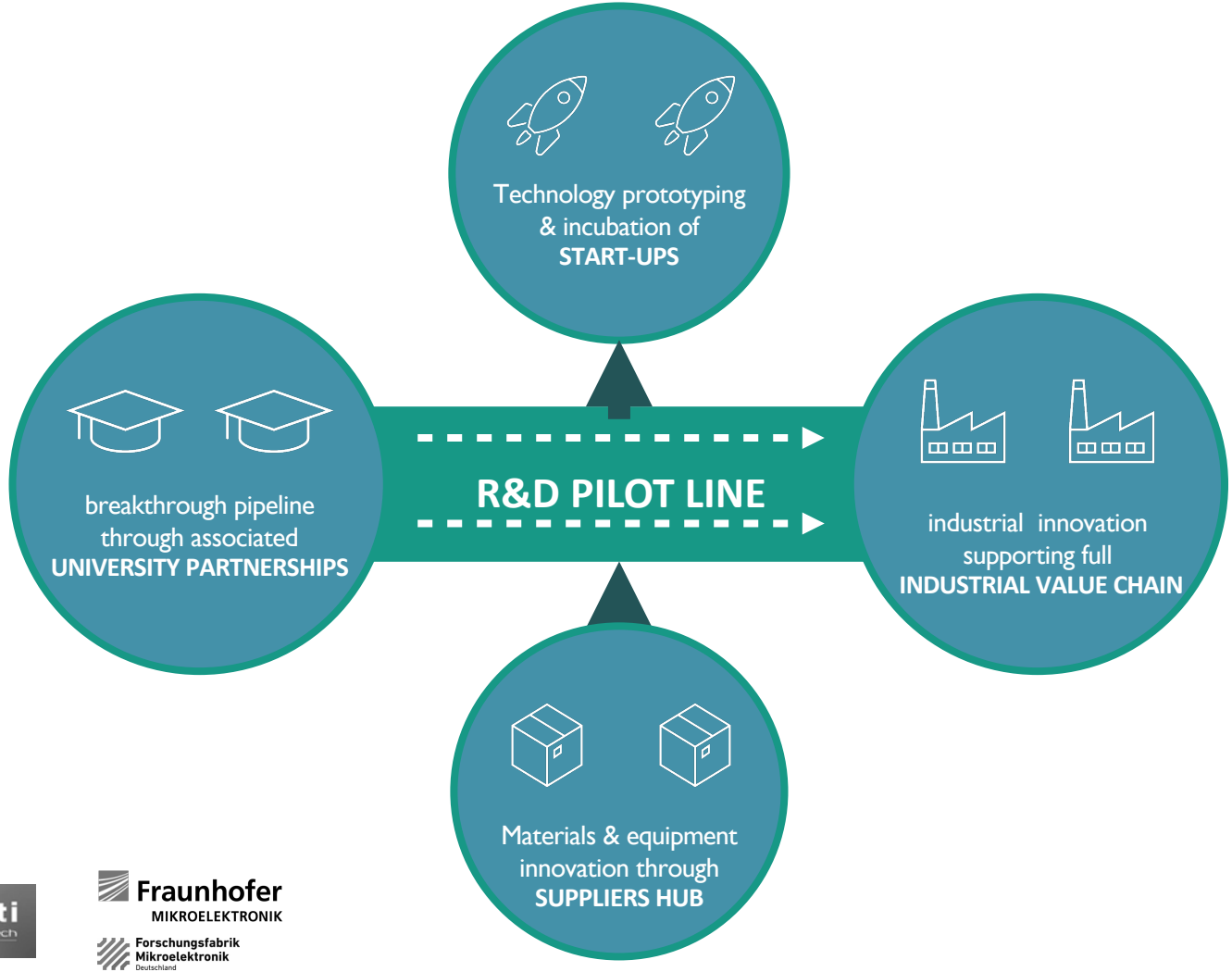

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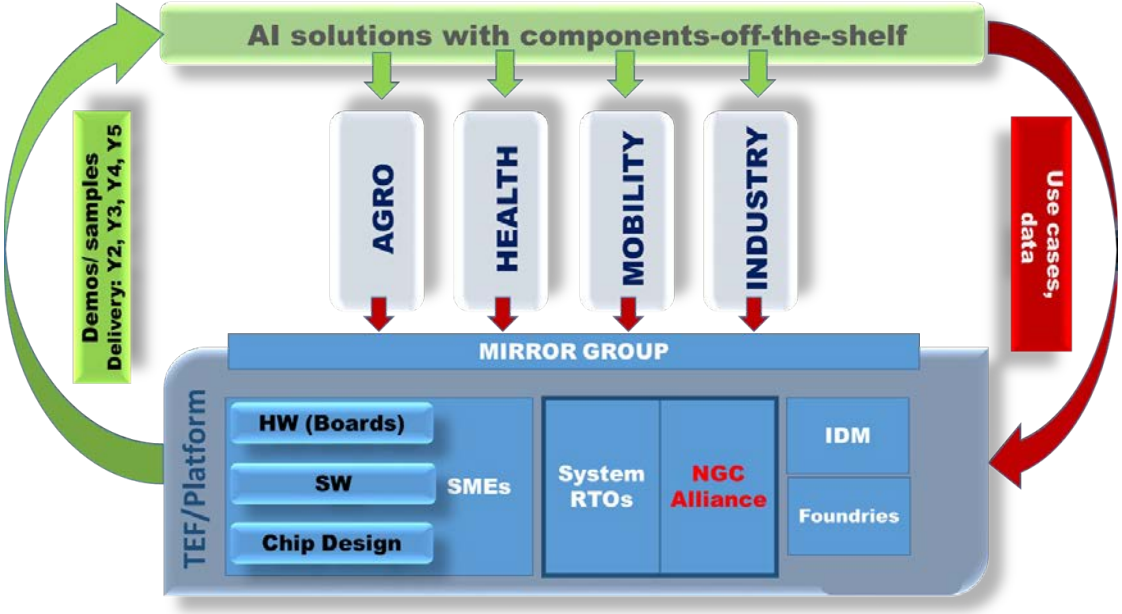
THE PREVAIL PROJECT AND VISION

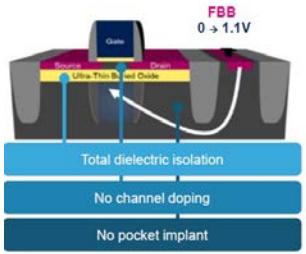


- The partners in the platform provide a set of 300mm technologies, open to any user, in order to fabricate prototype Edge AI chips (a few units) required by the user for non commercial purposes.
- Proposals are examined by the partners to verify feasibility, cost and delay.
- Proposals can come via DIH, KDT projects, directly.
- IP necessary for the execution and originating from the user remains his property and partners have access only for execution. The IP originating from the partners remains their property and, if necessary for exploitation, non-exclusive licenses will be provided. IP generated during the execution is property of the inventor.
- The user receives the prototypes and test them in its field of application.

FD-SOI 10nm

FD-SOI ideally suited for key markets

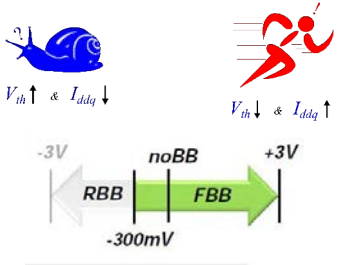
European FD-SOI ecosystem is a powerful engine of value creation

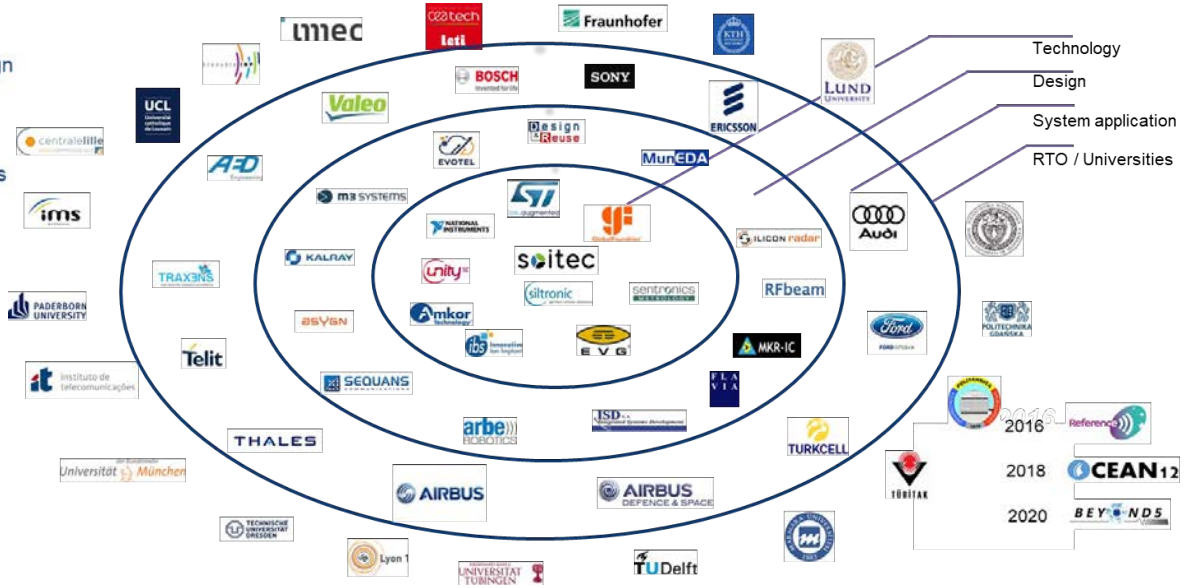


Power and energy efficiency

Analog performance
for mixed signal and RF design

Robustness
for mission critical applications





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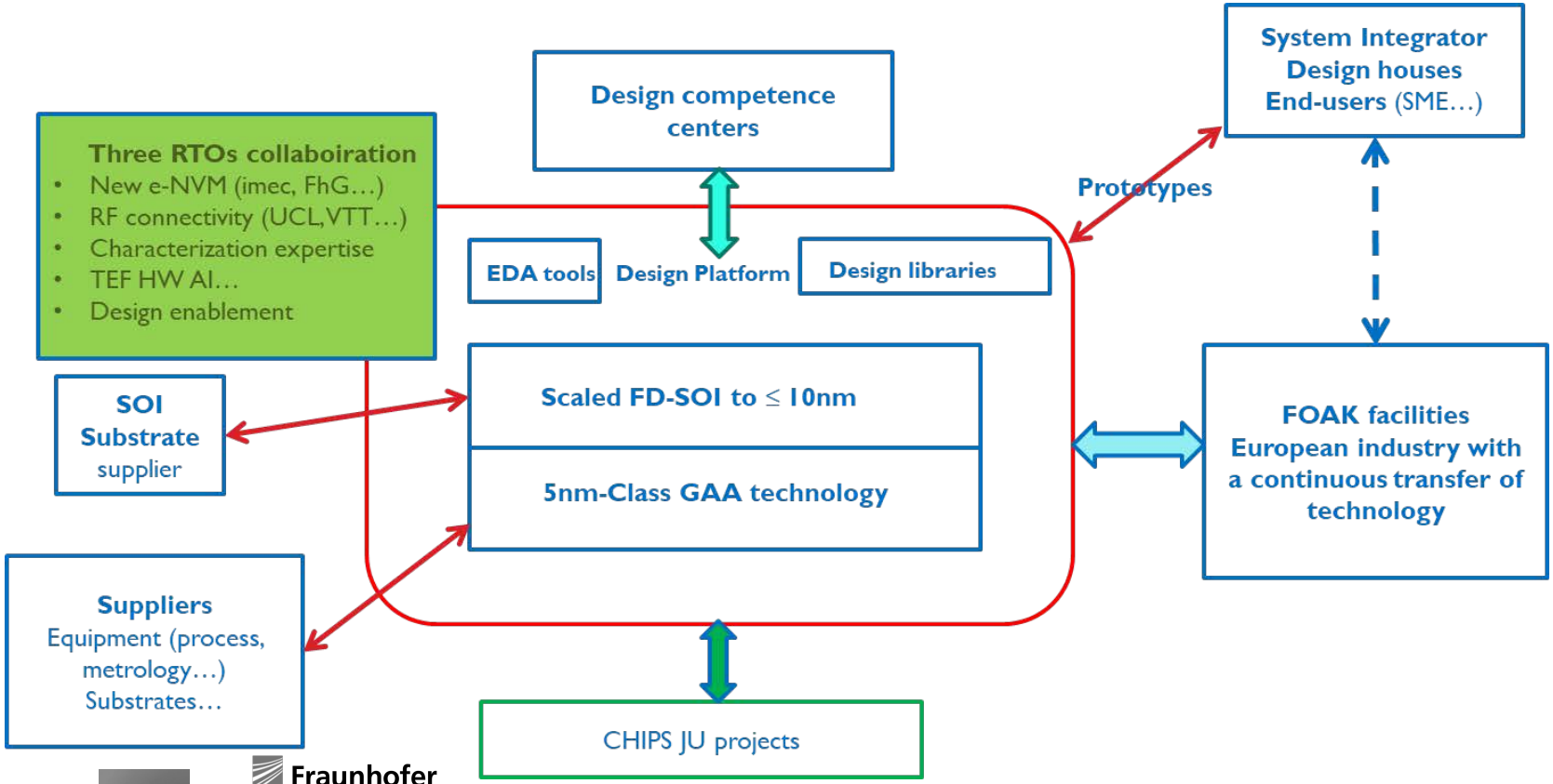
FD-SOI NEXT GEN pilot line concept: From the Lab to the Fab



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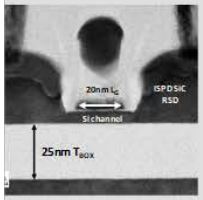
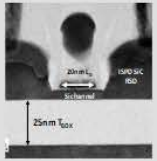
FD-SOI NEXT GEN (10-7 nm) pilot line

Current and near-future European FD-SOI offer

28nm FD-SOI | 22nm FD-SOI | 18nm FD-SOI





GF-Leti partnership

life.augmented → life.augmented

Current markets: MCU, Imagers, 5G/6G, IoT, RF, Wearables

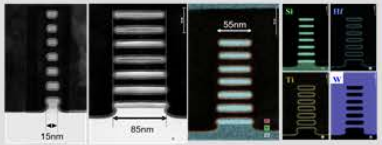
2022-2026 Technology Development FD-SOI 10-7nm

- Strained SOI wafer
- Carrier mobility boosters
- MEOL integration
- Embedded NVM
  - *MRAM by imec, FeRAM by FhG, OxRAM by Leti…*
- Full benefit of body-biasing
  - *EDA tools and IP*
- Process Design Kits
  - *provided to all European partners who want to test and evaluate technology*

2024-2027 Specific Development for key markets

- More-Than-Moore markets
  - *Automotive*
  - *5G/6G chips*
  - *RF Connectivity*
  - *Microcontrollers*
  - *IoT devices*
  - *Smart Imagers*
  - *Smart sensors*
  - *Cybersecurity*
  - *Wearables*
  - *…*
- Quantum
  - *Qubits on Si*
  - *CryoCMOS*

2026-2030 Breakthrough to nanowire/sheet technology



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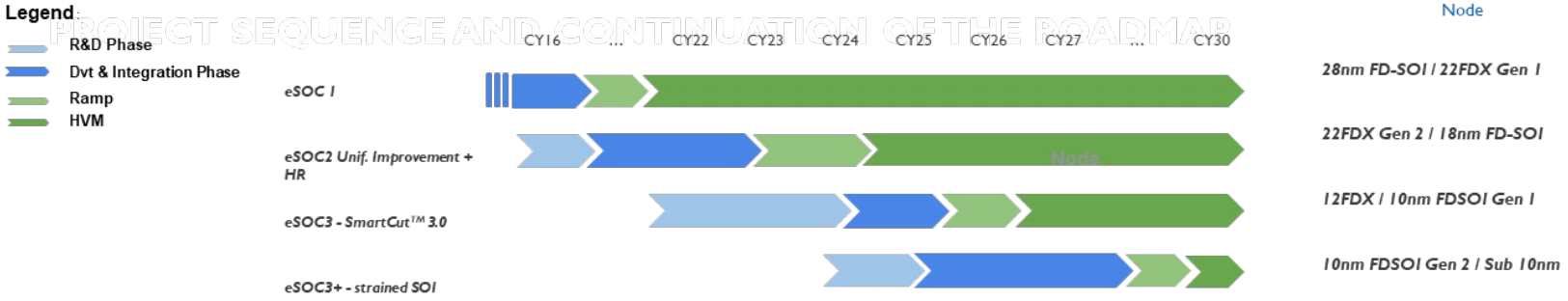
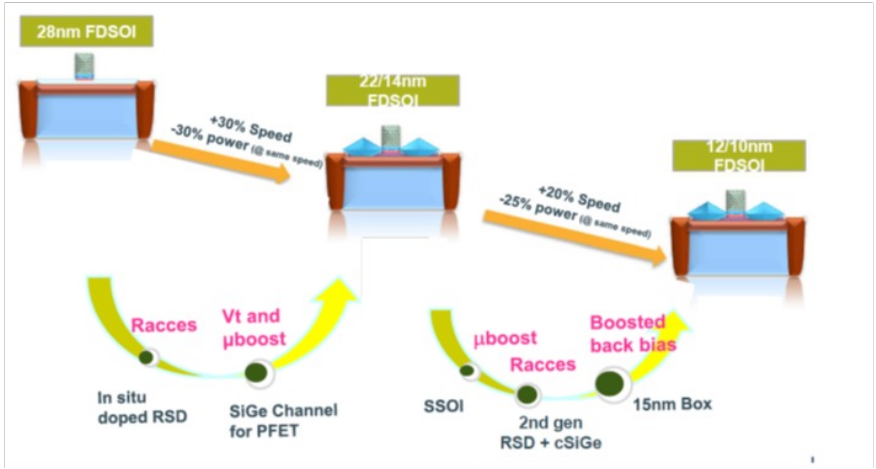
FD-SOI NEXT GEN Roadmap

Substrate



Node



Technology-Design

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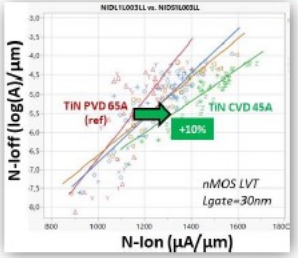
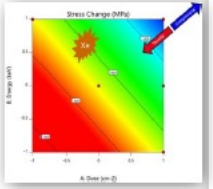
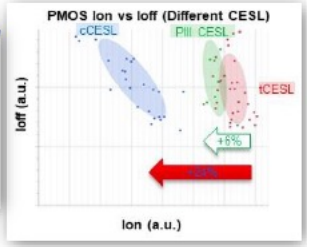
FD-SOI NEXT GEN Roadmap to 10-7nm

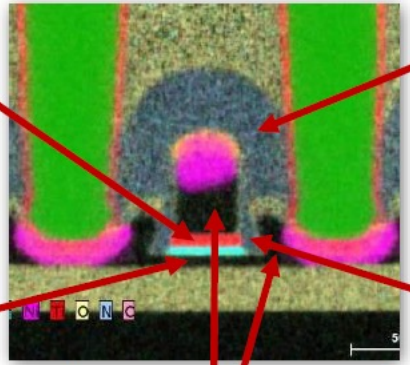
Gate stack
Material optimization



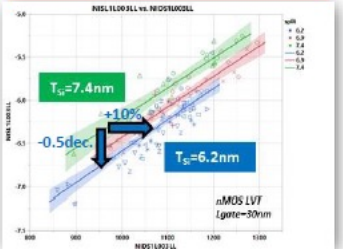
CESL
Inversed stress



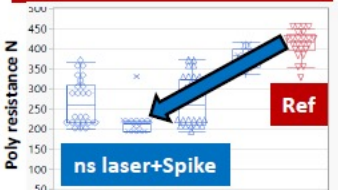




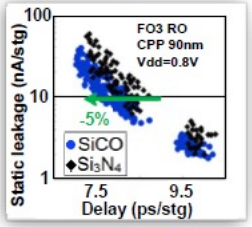
Channel engineering
Electrostatics control

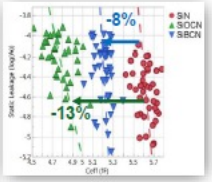


Laser anneal
Dopant activation



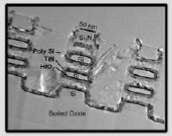
Low-k Spacer
Material optimization





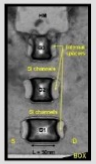
FD-SOI NEXT GEN: transition to GAA

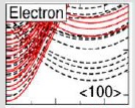
2006
Full 200mm processing route on GAA Nano-Beam stacked-channels
IEDM06



2008
NW with independent gates
IEDM08

2009
Inner spacer introduction
IEEE EDL 09

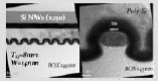




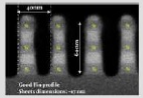
2013
GF Trigate NW Strain Booster
VLSI13

Full 300mm processing route

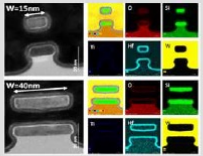
2014
Self-Aligned GAA transistors



2015
SIT/DSA Patterning

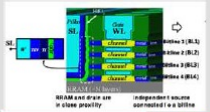


2016
GAA NS in a RMG process with inner spacer and SAC IEDM16



2019
Stress and strain evolution in stacked GAA transistors IEDM19

2020
IMC: 3D RRAM with GAA stacked-NS FET



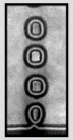
IEDM20

05 | 10 | 15

First patent

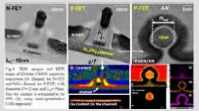
2006
French Ministry of Research RTB program

2009
ONO crystalline 3D Flash
IEDM 09



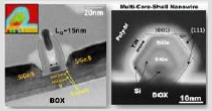
2011
13 crystalline levels

Micro Eng 11



2014
Dual-channel CMOS Co-Integration Si NFET and strained-SiGe PFET
IEDM14

2014
Epitaxial SiGe/Si Multi-(Core/Shell) P-FET Nanowire



IEEE TED 14
Paul Rappaport IEEE Prize

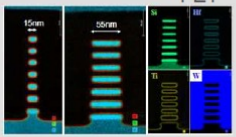
2013
Application of nanowires **to SET/SAT and quantum computing**

2016
LETI-NSP model For GAA MOSFET
IEDM16

2017
Perf. and design consideration for GAA FETs
IEDM17

2018
Application of nanowires **to sensing application**

2020
7-level-stacked Nanosheet GAA FET



VLSI20

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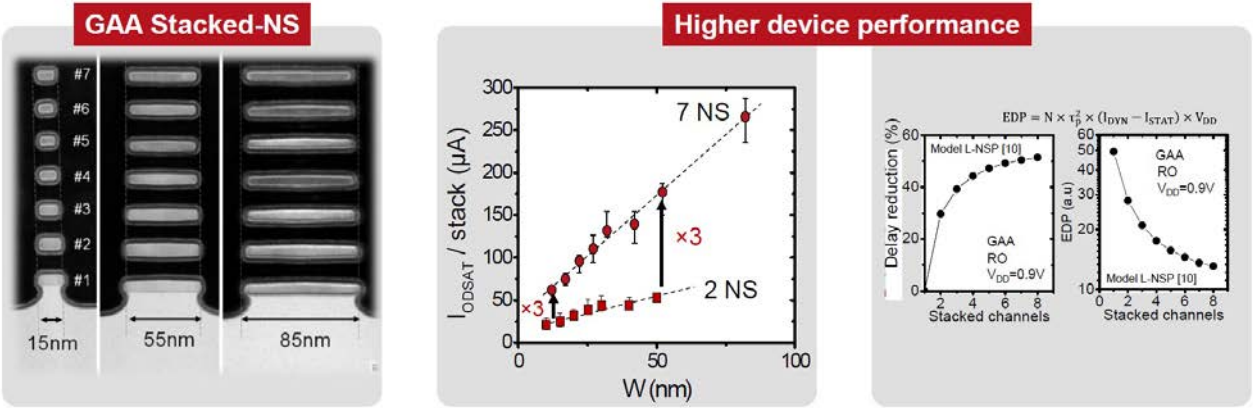
FD-SOI NEXT GEN Roadmap



Performance booster thanks to higher W_{eff}/footprint ratio

- Evolution of both FinFET and FD-SOI
- Flexibility performance/power
- Built on as follow-up of FD-SOI on the modules developed jointly in the advanced line in the earlier period.

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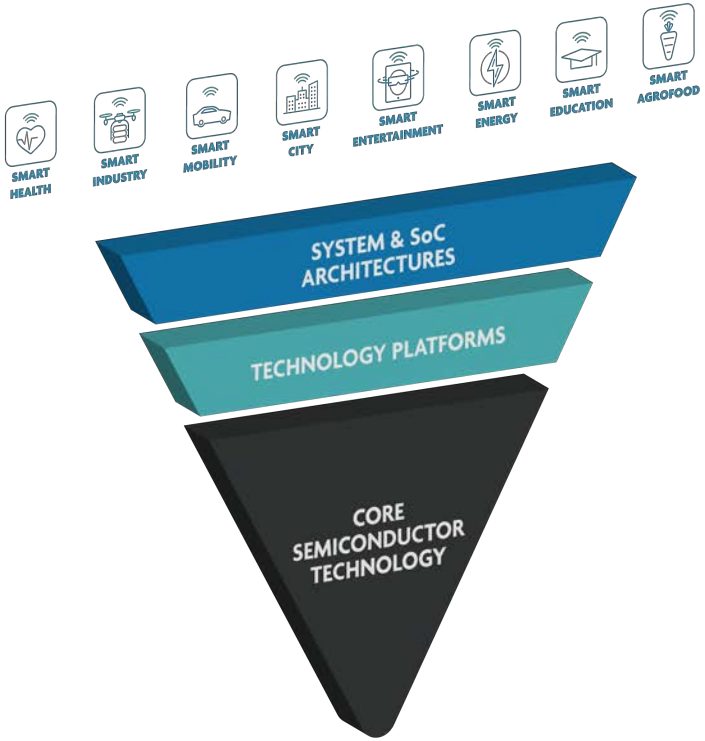
Leading edge and advanced semiconductor techology

Pan-European Pilot line structure



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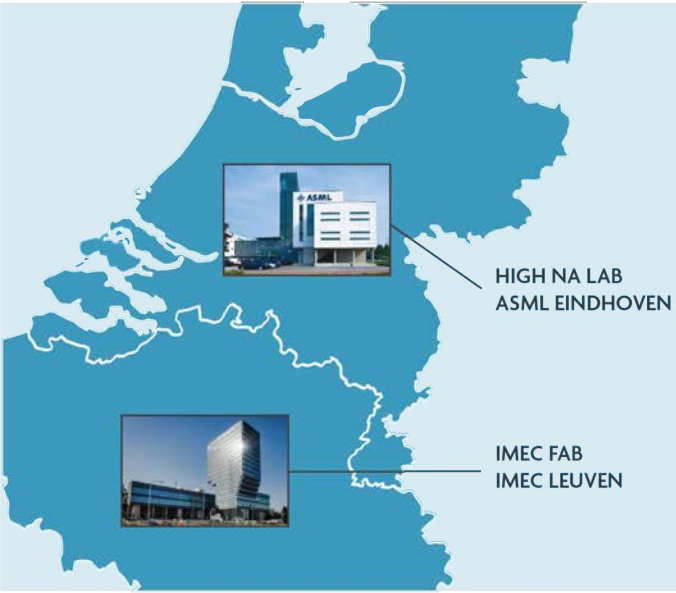
EXTENDED PILOT FAB



DEDICATED TEAM OF ASML-IMEC EXPERTS

ASML

- High NA EUV prototype
- Interface wafer track (TEL)
- Metrology (HMI, KLA)

Supplier ecosystem

Lam Research, TEL, ASM, ZEISS, SUSS MicroTec, KLA, brewer science, tok, ZEON, DNP, SCREEN, NuFLARE, synopsys, Mentor Graphics, SUMITOMO CHEMICAL

DONGJIN, Entegris, APPLIED MATERIALS, FUJIFILM, Inpria, Shin-Etsu, FRACTILIA, COVENTOR, PALL, Nissan Chemical, JSR, MERCK, TORAY TASMIT, Inc., Hitachi High-Tech, MITSUBISHI CHEMICAL MATERIALS

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Potential roadmap extension

	2018	2020	2022	2024	2026	2028	2030	2032	2034	2036
	N7	N5	N3	N2	A14	A10	A7	A5	A3	A2
Continued dimensional scaling										
Metal Pitch [nm]	40	28	22	21	18	16	16-14	16-12	16-12	16-12
Device and material innovations										
Metal Tracks	7	6	6	6	5	5	5	4	<4	<4
	FinFET	FinFET	FinFET	GAA Nanosheet	GAA Nanosheet	GAA Forksheet	GAA Forksheet	CFET	CFET	CFET Atomic
Context-aware interconnect										

System-technology co-optimisation

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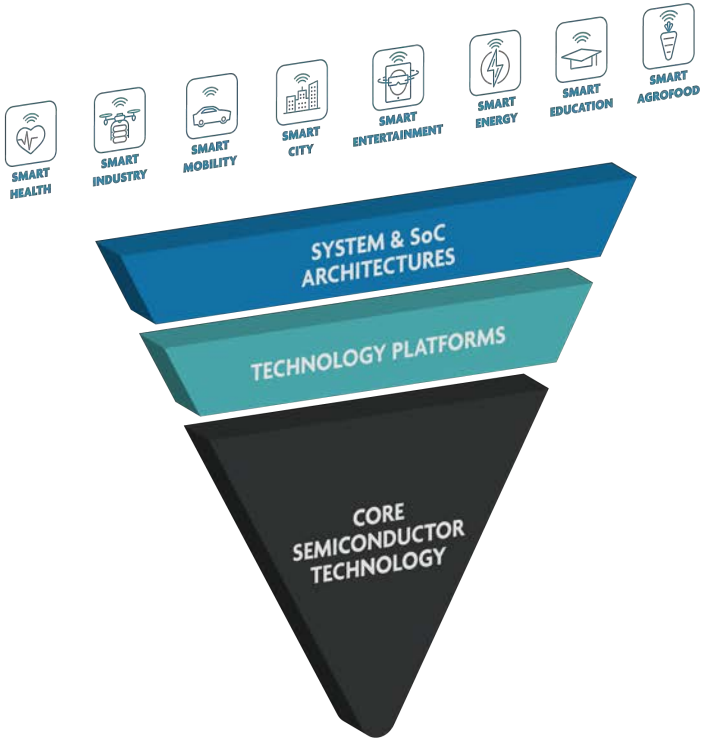
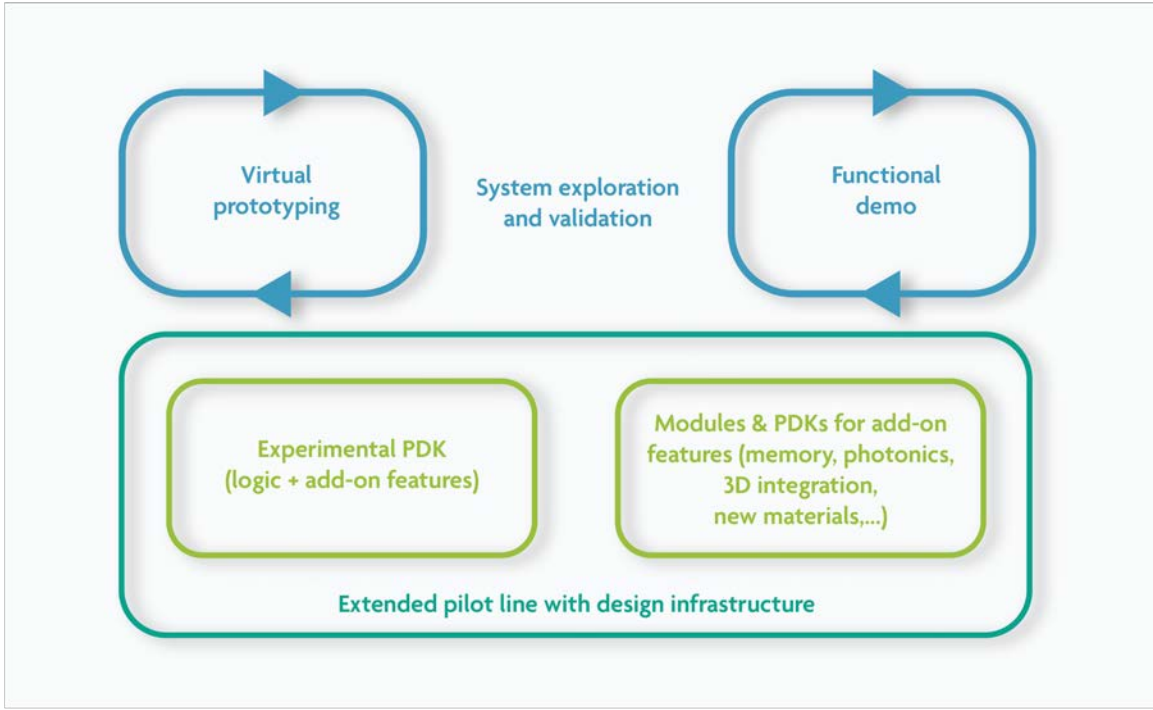
Pan-European Pilot line structure





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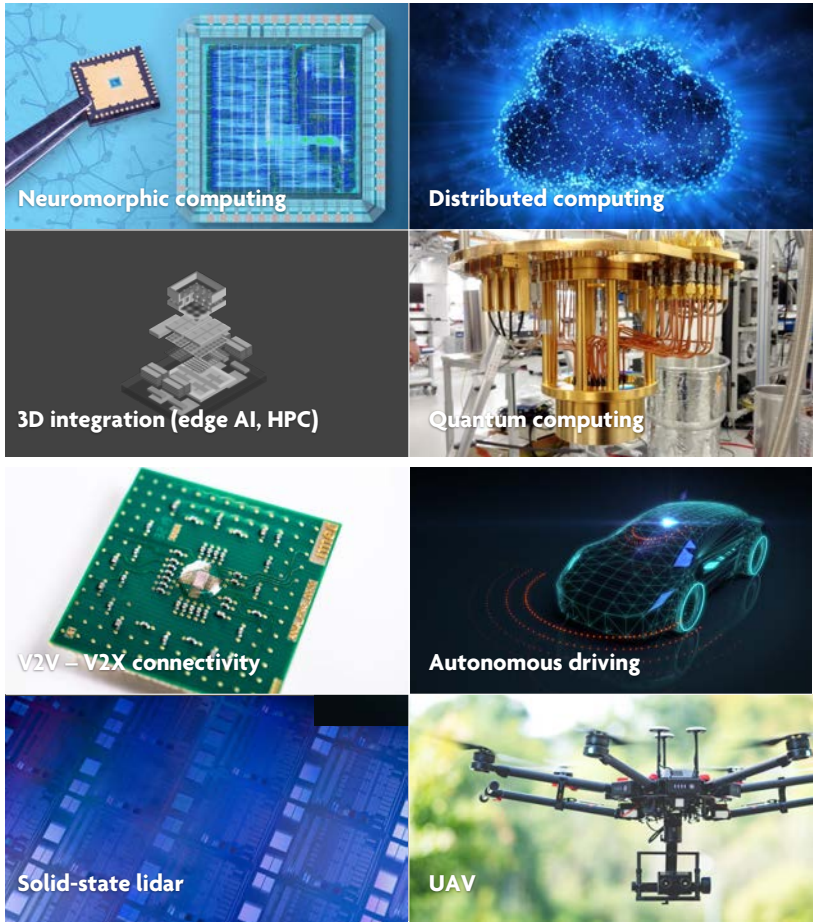
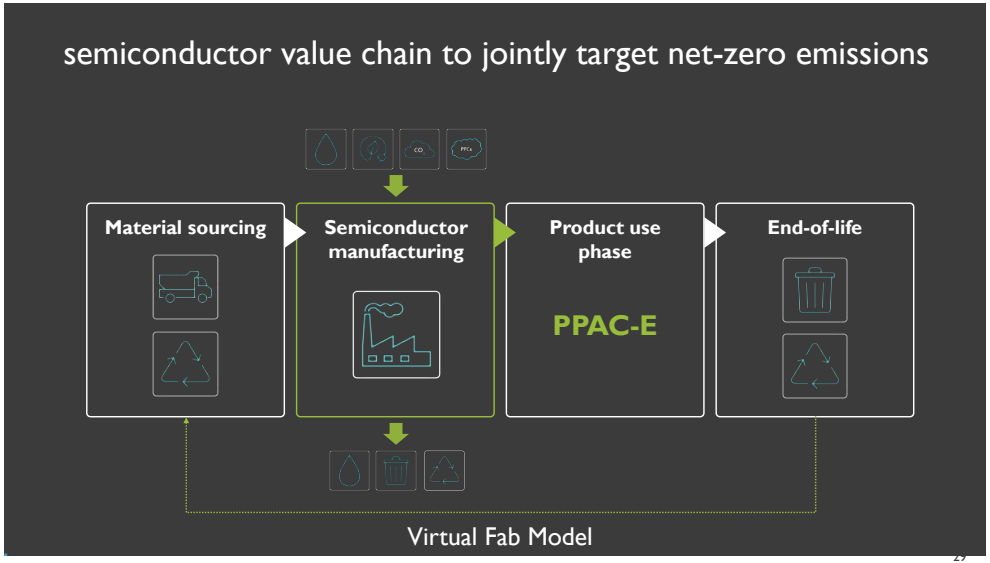


Enabling functional demonstration for various application domains

Driving innovation for net-zero emission.



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Advanced Heterogeneous System Integration

Advanced Heterogeneous System Integration

Narrative

- Challenges in our modern world need new functionalities, new technologies and new applications
- Moore's law will be "carried" by heterogeneous integration
- Heterogeneous integration offers the possibility of re-assembling different technologies
- New functionalities become possible by new packaging technologies
- Packaging technologies use more and more frontend equipment (Scanners, CMP, ...)
- The value add of packaging increases tremendously
- There are limited manufacturing possibilities in Europe which would process low-mid packaging volumes
- A new approach to packaging, involving the value chain, is needed

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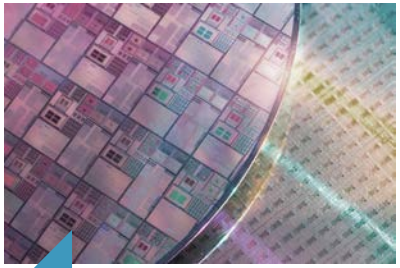
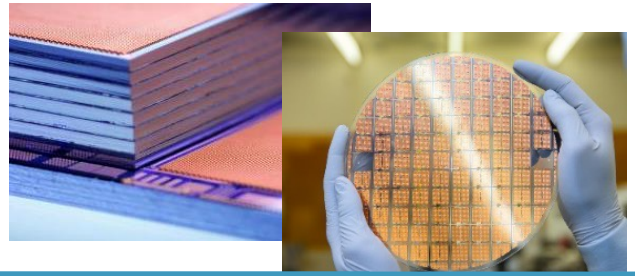
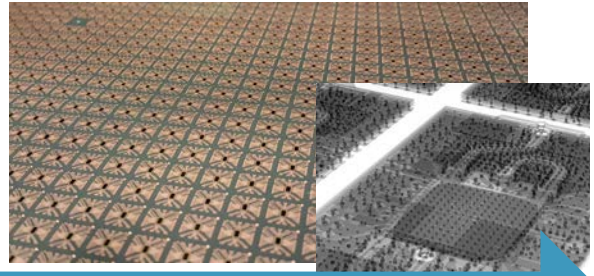
Fraunhofer – Heterogeneous Integration

From Wafer Level System Integration to Panel Level System Integration







CMOS Feature Sizes
5 nm … >100 nm

WLP Feature Sizes
0.75 µm … >10 µm

PLP Feature Sizes
< 5 µm … 100 µm

Wafer Level Packaging (WLP)

Technology: Based on thin film materials & equipment
Wafer size: … up to 300 mm
Input: CMOS / III/V / WBG wafers
Output: 2.5D/3D integrated systems or system components

Panel Level Packaging (PLP)

Technology: Based on PCB materials & equipment
Panel size: up to 610 x 456 mm²
Input: CMOS / III/V / WBG dies (w/ bumping)
Output: Packaged/embedded modules

FMD Pilot Line – Advanced Heterogeneous System Integration

Low Volume Production – High Quality High Value Chips

FMD Pilot Line – Advanced Heterogenous System Integration (AHSI)

Module Chip-Design

- Design Enablement
- Circuit Design
- Design for System Integration

Module Next Generation Power

Module Advanced Silicon Solutions

Module RF / Optoelectronics

Module Advanced Packaging

- Multiple materials / components / subsystems
- High precision assembly
- High density substrates
- Chiplets

Module Characterization, Test & Reliability

Markets, Customers, Application Industry

- Automotive
- Aerospace
- IDMs and Foundries
- Health
- Energy
- Consumer
- …

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FMD Pilot Line – Advanced Heterogeneous System Integration

Interaction with partner technologies

CEA-Leti-Pilot Line: Advanced Nodes , 10nm SOI, 5nm GAA
Imec-Pilot Line: Advanced Nodes, < 2nm, specialties & SoC

FMD Pilot Line – Advanced Heterogeneous System Integration

Module Chip-Design

Module Next Generation Power

Module Advanced Silicon Solutions

Module RF / Optoelectronics

Module Advanced Packaging

Module Characterization, Test & Reliability

Available Commercial Technologies e.g. EU, US, Asia

Markets, Customers, Application Industry

- Automotive
- Aerospace
- IDMs and Foundries
- Health
- Energy
- Consumer
- …

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Summary

Pan European Pilot Line Facility – New value to the Innovation System

Win-Win-Win towards a long-term advantage for Europe

Stakeholder	Value Offering
Chip foundries	• Predevelopment of technology modules • Access to design services to create foundry business • Outsource handling of prototype runs / small volume business
Integrated Device Manufacturers	• R&D services, focus on transferability into commercial production lines • Use of advanced heterogeneus system integration for creating new products and business offerings • Options for insourcing of high innovative products with volume forecast • Design services for IDM's new chips
Semiconductor Customer	• Easy access to specialized technologies for high complexity products • Use of advanced heterogenous system integration for creating new products and business offerings • Proof of Concept, demonstrators with high TRL / low volume production, • Scale up into commercial technologies commensurate with market growth
Research Community	• Access to extended technology capabilities in research cooperation • Support of transfer of research results into applications
Start-up	• Access to special technology • Prospect to create technology start-up without own cleanroom

Semiconductor Customer: building products based on semiconductors
Semiconductor Manufacturer / Semiconductor FABs: design up to production of semiconductors

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