



Chips for Europe Initiative

Colette Maloney

Marco Ceccarelli

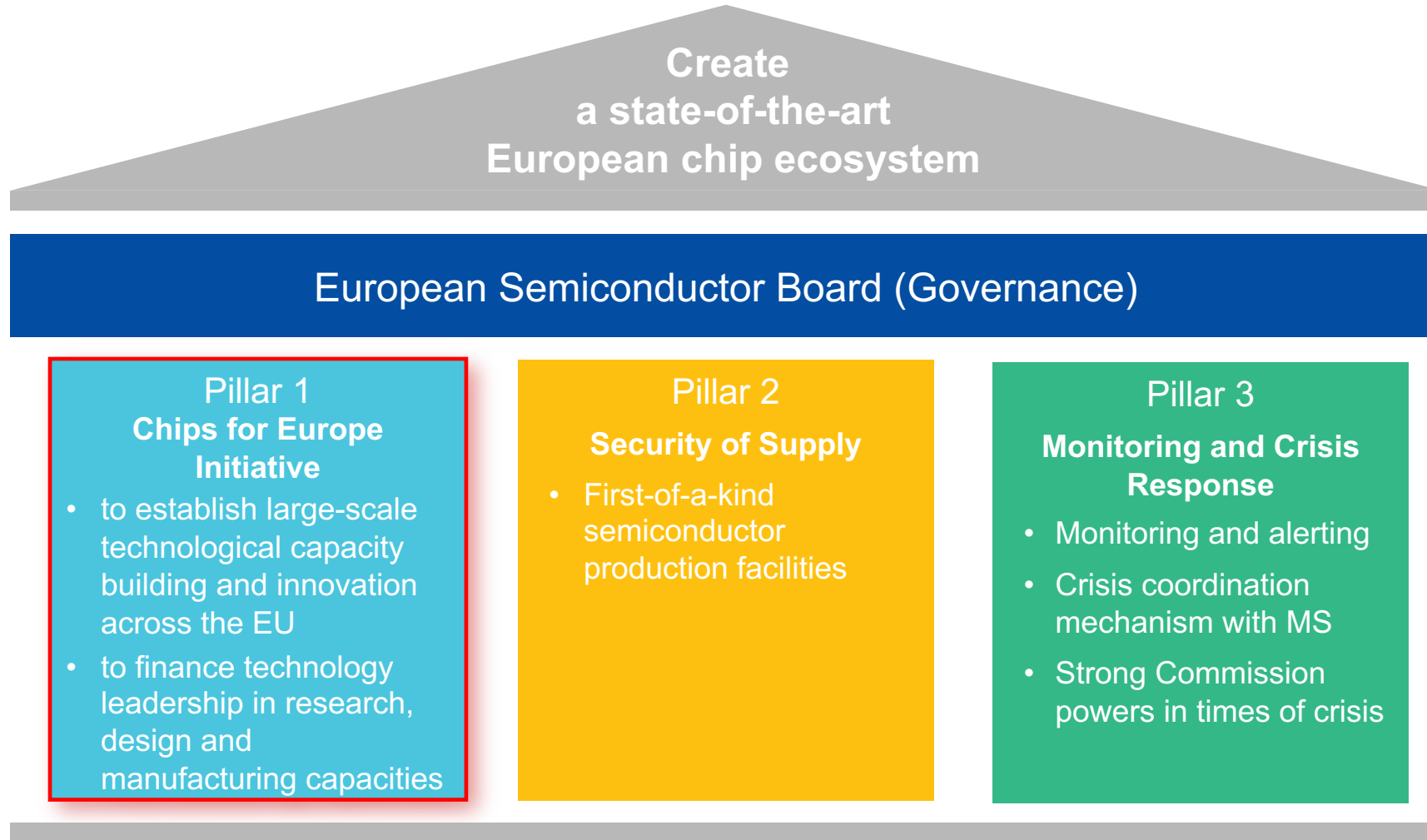
Francisco Ibañez

EC DG CNECT

ECS Brokerage event

Brussels, 7-8 February 2023

Three pillars of the Chips Act



Chips for Europe Initiative

Rationale for the Initiative



Situation today

- EU is strong in R&D, RTOs and in manufacturing equipment
- R&D supported by EU and Member States with ~4 B€ in MFF programmes

What is the EU missing

- Capability for translating R&D excellence into new markets
- Industrial capabilities in leading-edge design and manufacturing
- Market pull



- EU + MS programmes cover R&D and innovation
- Measures to help **bridge the gap to market** are required

Chips for Europe Initiative

Aim: bridging the gap from lab to fab

5 Objectives

- 1 Reinforce design capacity by providing a **virtual design platform**
- 2 Enhance existing and developing new **pilot lines**
- 3 Accelerate the development of **quantum chips**
- 4 Expand **skills** and set up a network of **competence centres**
- 5 Facilitate SME access to **equity and loans** through a dedicated **Chips Fund**

Chips JU

EIC
I-EU

Basic
Research

Applied
Research

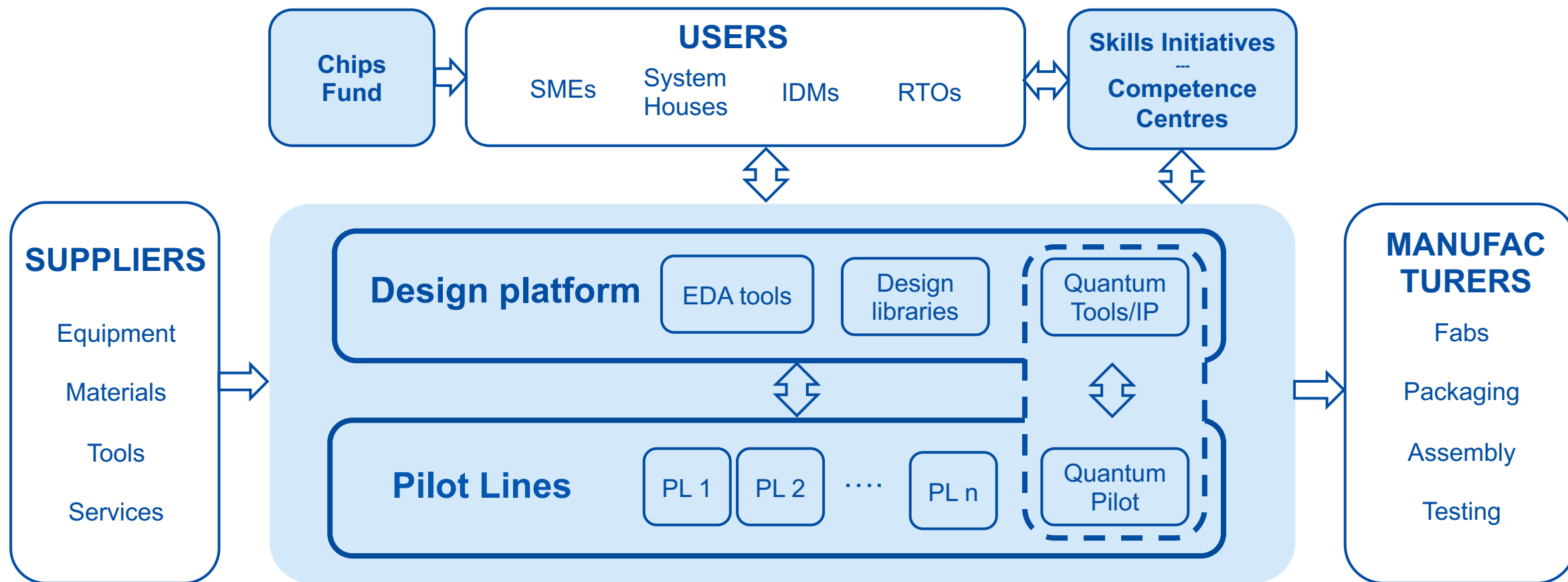
Prototyping

Pilot lines

Production

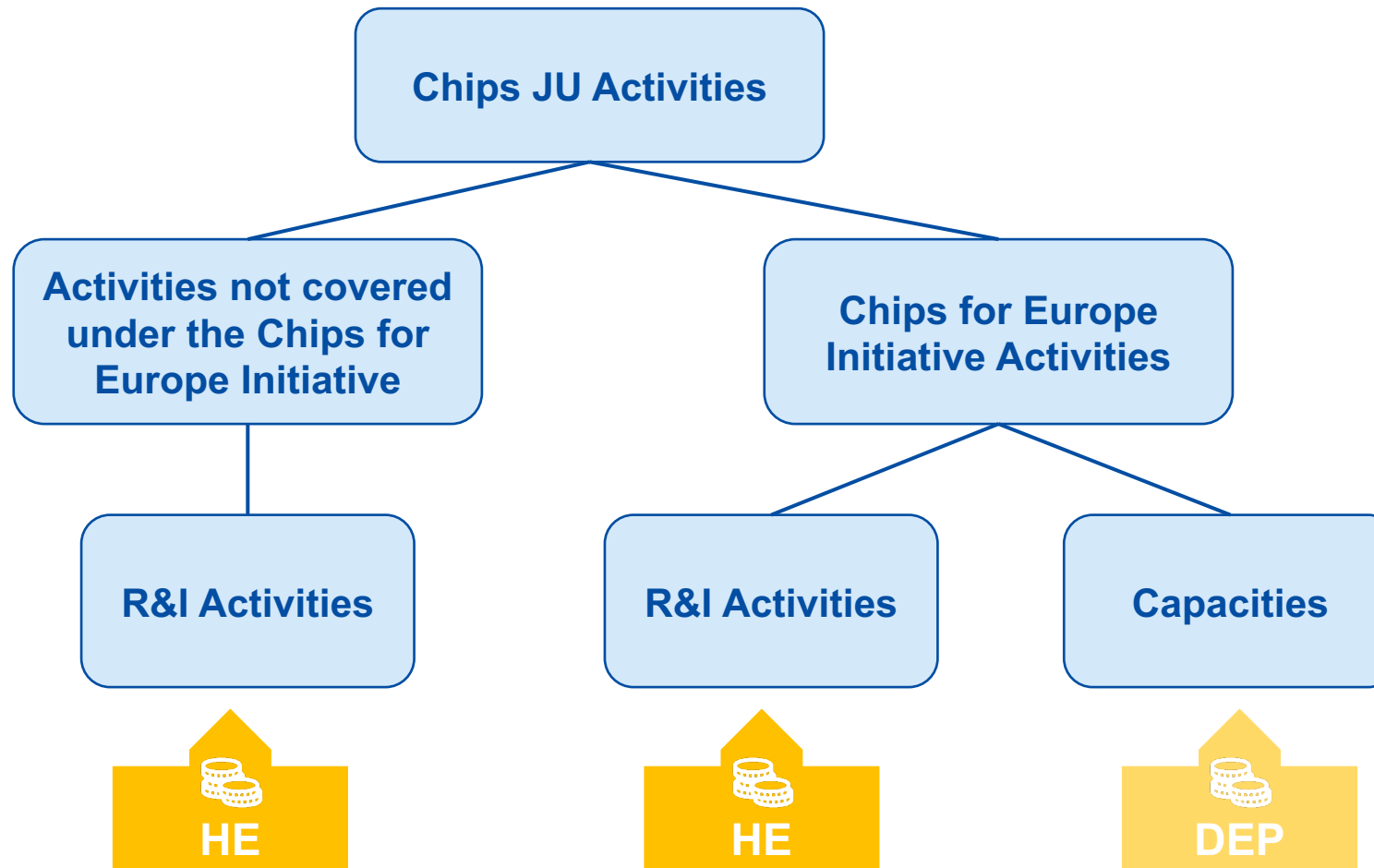
Chips for Europe Initiative

Bridging the gap from lab to fab



Future “Chips JU” Activities

Chips for Europe Initiative



Programme execution ensuring long-term operations



ECIC - EU Chips Infrastructure Consortium
proposed **legal instrument** for funding Chips for Europe Initiative actions

- **Legal personality**: can exist beyond the lifetime of MFF and JU, with full amortization of CapEx => simplified access to funding
- Accommodate **financing** from different sources, including **loans**
- **Voluntary** instrument, participation of entities from at least **3 MS**
- Support **flexible** implementation: duration, consortium, MS participation, IP management

Design Platform

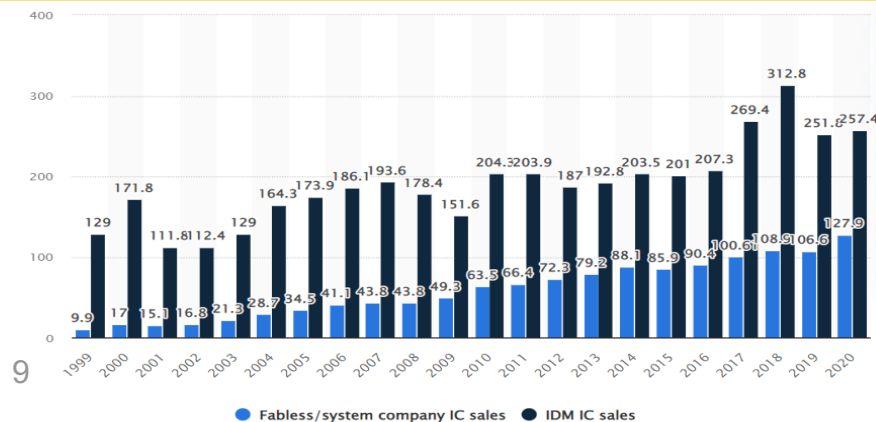
Design Platform

Problem statement

The market



- Design represents nearly 1/3 of the market of semiconductor value chain
- Fabless companies grow fast: 2.7x in 10 years - now 35% of the market
- Large system companies engage in design to capture value by verticalization



In Europe



- Design capacity mostly with IDMs - share of fabless declined in 10y from 4% to 1%
- High entry/scaling barriers, limited funding => valley of death
- Limited skills on advanced nodes
- Low level of engagement in chip design by system companies

Design platform - scope



Ambition

Foster the development of the semiconductor **design ecosystem** in EU, reinforcing capacity to innovate and create European Intellectual Property through IC design

Main scope

- **Reduce entry barriers** and admin burden for EU companies engaging in chip design
- **Facilitate access** to pilot lines and manufacturing facilities
- Foster **collaboration** among EU stakeholders, also on new IP and tools (incl. open-source, quantum)
- **Access** to network of **competence centers** offering **training** and support to boost design skills

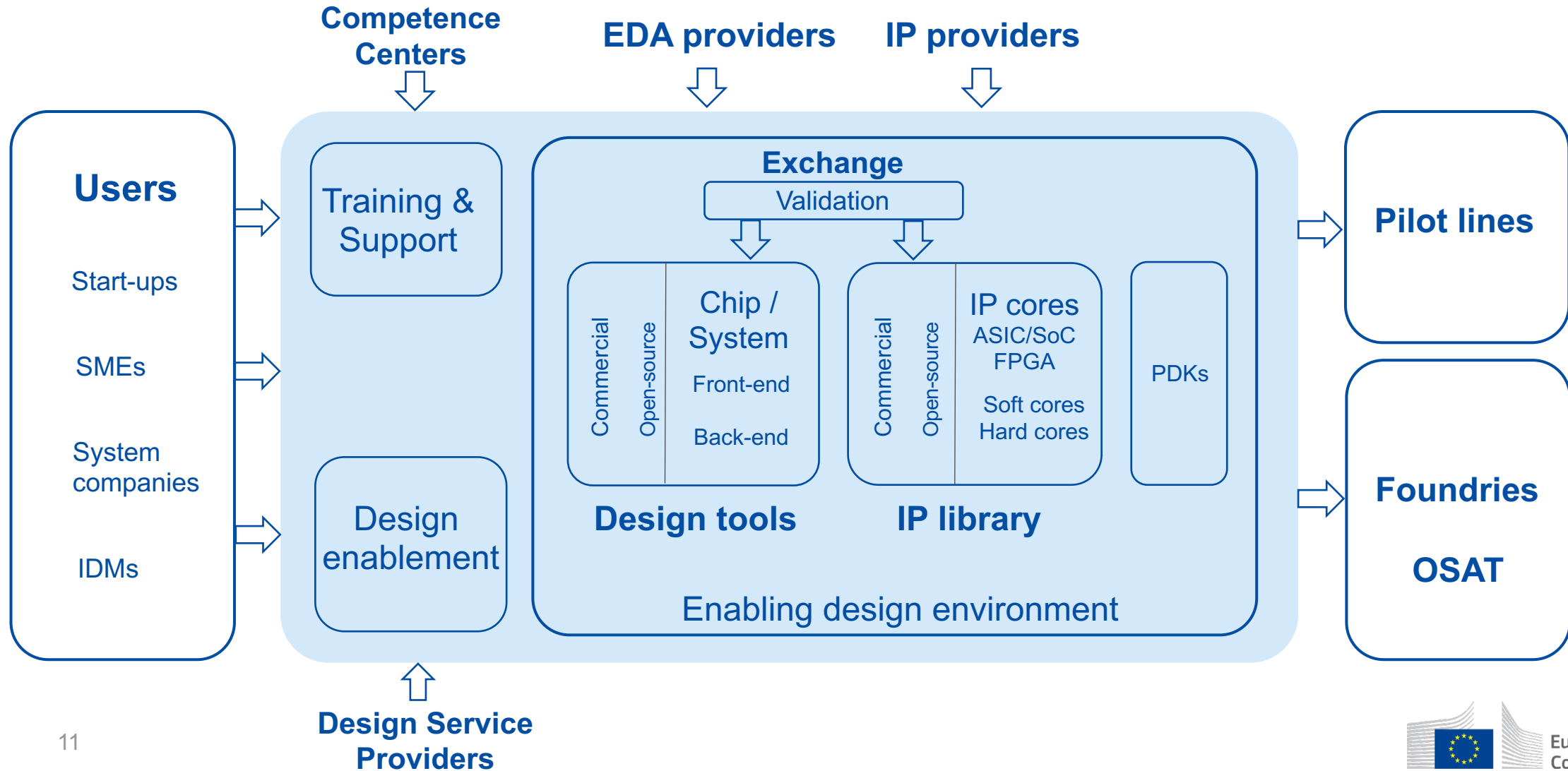


Instrument



Develop a **virtual design platform**, offering **cloud-based** access to tools, libraries and support services to accelerate development and reduce time-to-market

Design platform

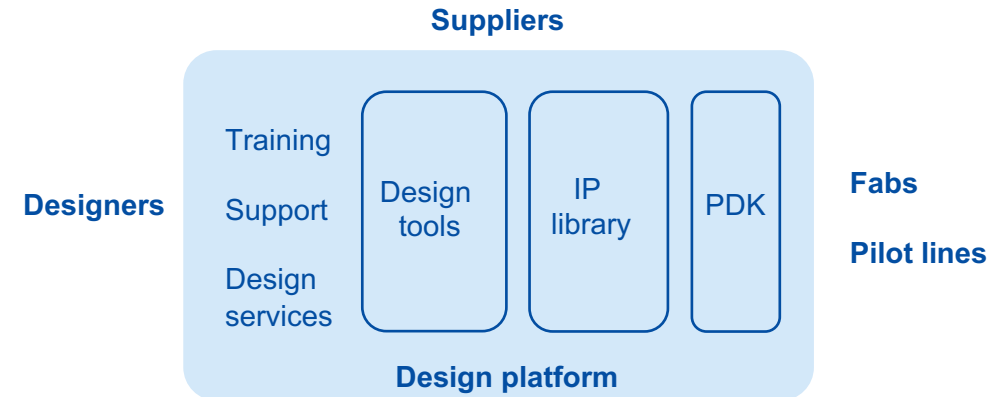


Design platform Model

Added value



- Easy access on the **cloud**
- No upfront CapEx for on-premise IT **infrastructure**
- Maximum computing **scalability** for simulation and verification
- High level of **security**, fully audited
- Verified **interoperability**
- **Streamlined process** with framework agreements
- Access to virtual **prototyping**, **MPW** and foundry services



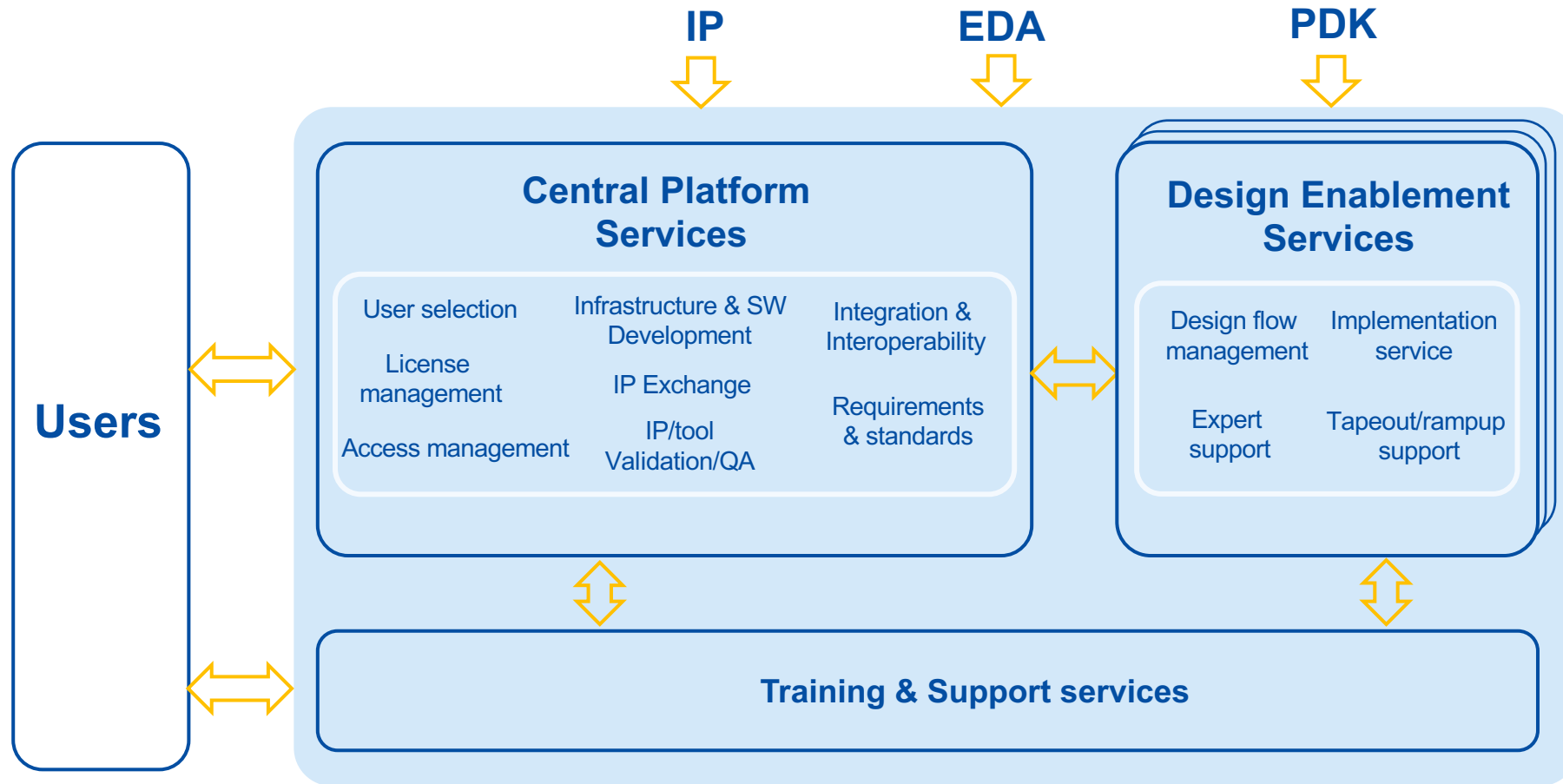
Key partners



- **Foundries**, **IP** vendors, **EDA** and **infrastructure** providers - collaboration for **secure cloud** solution
- **ASIC/SoC design services** for design enablement, workflows
- **Competence centers** offering training to address **skills** gap

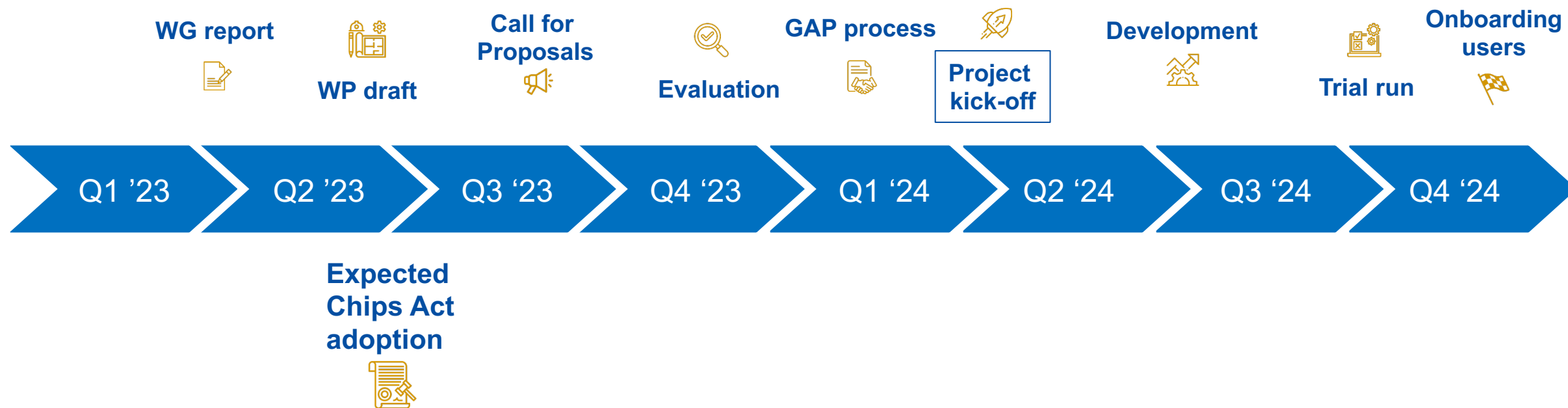
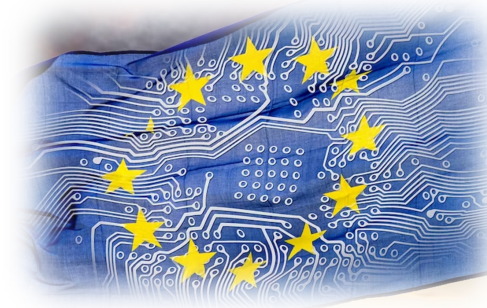
Design platform

Possible functional implementation (Work in Progress)



Design Platform

Draft Planning*



Pilot lines

Semiconductors R&I challenges

EU semiconductor ecosystem: capability to convert **excellent research** into **industrial innovation** is limited

- Efforts are **fragmented** across technologies, value-chain segments and member states
- Current **instruments** cannot provide a path for sustainable research **from the lab to industrialisation**
- We have **leading research organisations** but their outcomes are **not always taken up** by EU companies
- Chip development is **costly and risky**, particularly in early stages of new technologies
- Opportunities in **emerging trends** not always seized on time

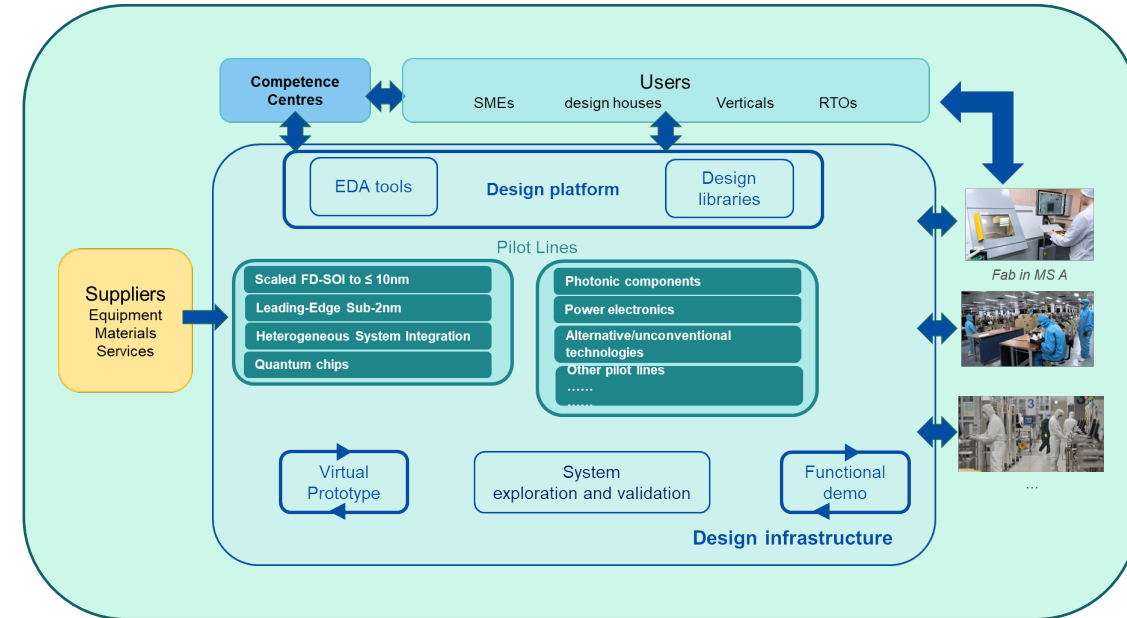
Pilot Lines can be the response to these challenges

Pilot lines in the Chips Act

Goal

To establish a Pilot Line Infrastructure consisting of

- a set of new pilot lines that will play a central role, such as
 - *Scaled FD-SOI down to 10nm and below*
 - *Leading-edge process technology at 2nm and below*
 - *Advanced Heterogeneous System Integration*
- a set of new and existing pilot lines that will be established or upgraded to integrate complementary competences
- a link with the design platform as well as the whole ecosystem, including competence centres

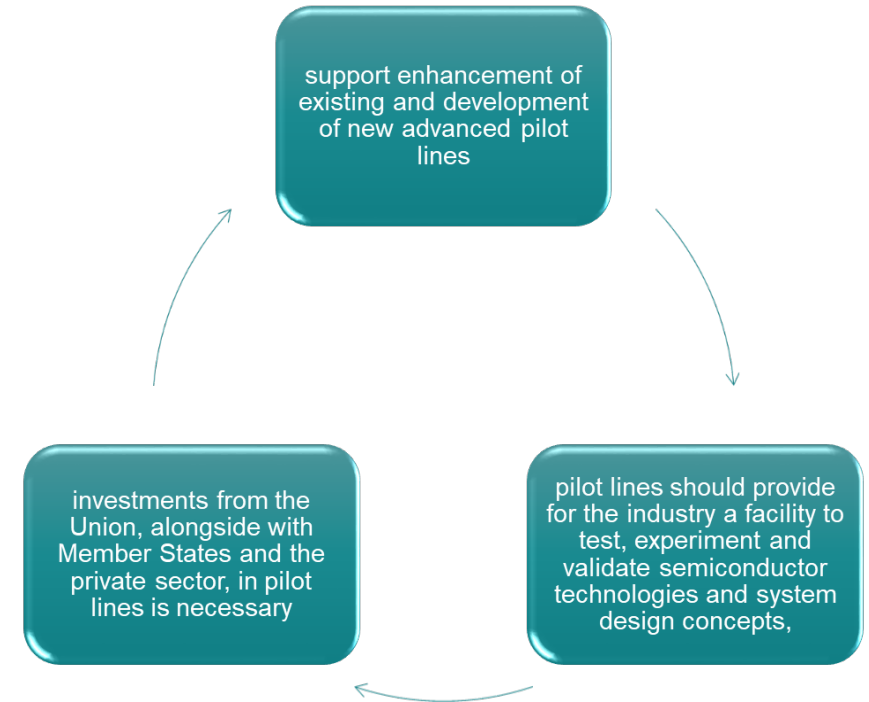


General Approach

Council position (1st Dec. 2023)

Operational objectives of the Chips for Europe Initiative:

ii) to provide the basis for strengthening the security of supply and the semiconductor ecosystem in the Union, the Initiative should **support enhancement of existing and development of new advanced pilot lines** to enable development and deployment of cutting-edge and next generation semiconductor technologies. **The pilot lines should provide for the industry a facility to test, experiment and validate semiconductor technologies and system design concepts**, while reducing environmental impacts as much as possible. **Investments from the Union, alongside with Member States and the private sector, in pilot lines is necessary** to address the existing structural challenge and market failure where such facilities are not available in the Union hindering innovation potential and global competitiveness of the Union



Pilot Lines

Take aways from consultation workshops

- **Essential elements:** leading-edge technology, industrial relevance, user requirements, industrialization plans, pan-EU,
- **Pilot line models.** From R&I to manufacturing, service provision, test and experimentation
- **Scope.** Microelectronics & photonics, process technologies: front end, back end, system integration,...
- **Timing.** Compatible with technology roadmaps
- **Implementation.** Appropriate support instrument (sustained R&I, flexible consortium, combined financing,...)
- **Consortium.** Multiple competences, partner interactions, SME involvement,...
- **Users.** Involvement, application/technology matching, support risk-taking
- **Access conditions.** Open, non discriminatory, cost efficient
- **Technology maturity.** TRL and MRL approaches
- **Standards.** Trusted chips, green chips
- **Skills.** Contribution of pilot lines to on-the-job training, mobility of researchers
- **Access to finance.**
- Linking Pilot Lines to the **Design Platform.** PDK, ADK, prototyping, experimentation...

Implementation of Pilot Lines Timeline*

Phases

1. Invitation to pilot lines hosting organisations (2Q2023)
2. Call for proposals (3Q2023)
3. Launch of first batch (1Q2024)

Other considerations

Participants, implementation, financing, ...

** Based on current estimation of the legislative process*

Skills & Competence Centres

Skills - ongoing activities



2023 Year of Skills - announced by EC President von der Leyen in SOTEU 2022

- **Pact for Skills**, part of the European Skills Agenda:
 - the Large-Scale Partnership in Microelectronics is one of the first launched in 2020;
- **Digital Education Action Plan 2021-2027**:
 - boosts digital skills of citizens, preparing graduates for the labour market
- **Digital Skills and Jobs Platform** providing access to information on digital skills, funding, training and jobs
- **Structured Dialogue** with MS to make digital education effective and inclusive
- **Erasmus+ - Sectoral cooperation on skills – Microelectronics**
 - The **METIS** project provides data, best practices and online courses for skill upgrades in Microelectronics
 - The **EcoVem** project with VET centres, technology universities, industry, social partners for excellence in Microelectronics
- **Digital Europe Programme – SO4 on Digital Skills**
 - 3 calls have recently closed for: 1- education programmes on digital technologies, 2- upskilling and reskilling, 3- University curricula and mobility

Skills in the Chips Act



Workshop on skills – held on 2 December 2022 with EC, MS, industry, University, training centres, to discuss necessary actions to address the skills gap in semiconductors in EU

- **Chips JU** will have dedicated calls, in collaboration with Member States, for:
 - Public awareness campaigns
 - Scholarships and Traineeships
 - Free training, upskilling and reskilling programmes
 - Training and support programmes for SMEs
 - Link with complementary mobility under Erasmus+
- A **DEP call** on the above topics is already foreseen in Q3 2023
- Many actions will be coordinated by the **Competence Centres**

Competence Centres



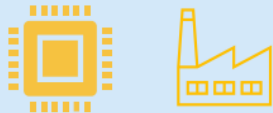
EU support for at least one
centre per Member State



Co-investment with
Member States and
Regions



Supporting industry
and public services



Access to design
platform and pilot lines



Focus on
Semiconductors
Skills



A strong European
network of Competence
Centres

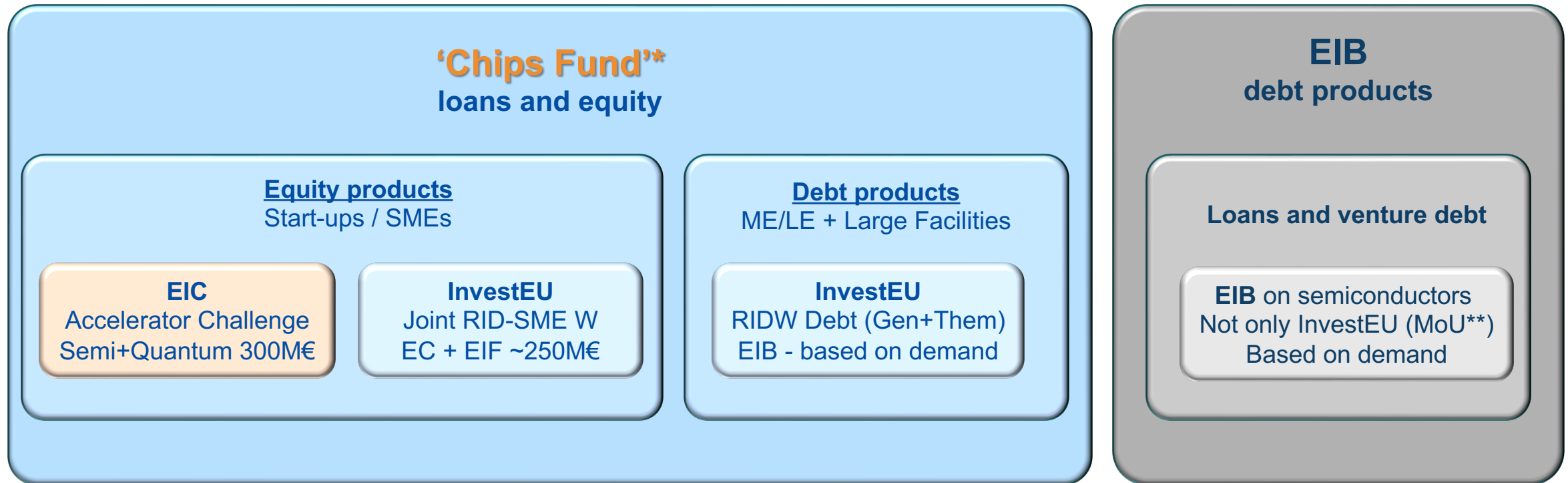
Competence Centres



- Address the **skills shortage** by offering access to **training**, including workforce upskilling and reskilling, on semiconductors
- Facilitate effective use of capacities and facilities of the Chips for Europe initiative, including access to **design platform** and **pilot lines**, **funding** opportunities etc.
- **Connect** stakeholders to national and international programs, and resources linked to semiconductors
- Act as **access point** to the **network** of competence centres

Chips Fund

The “Chips fund” investment facility

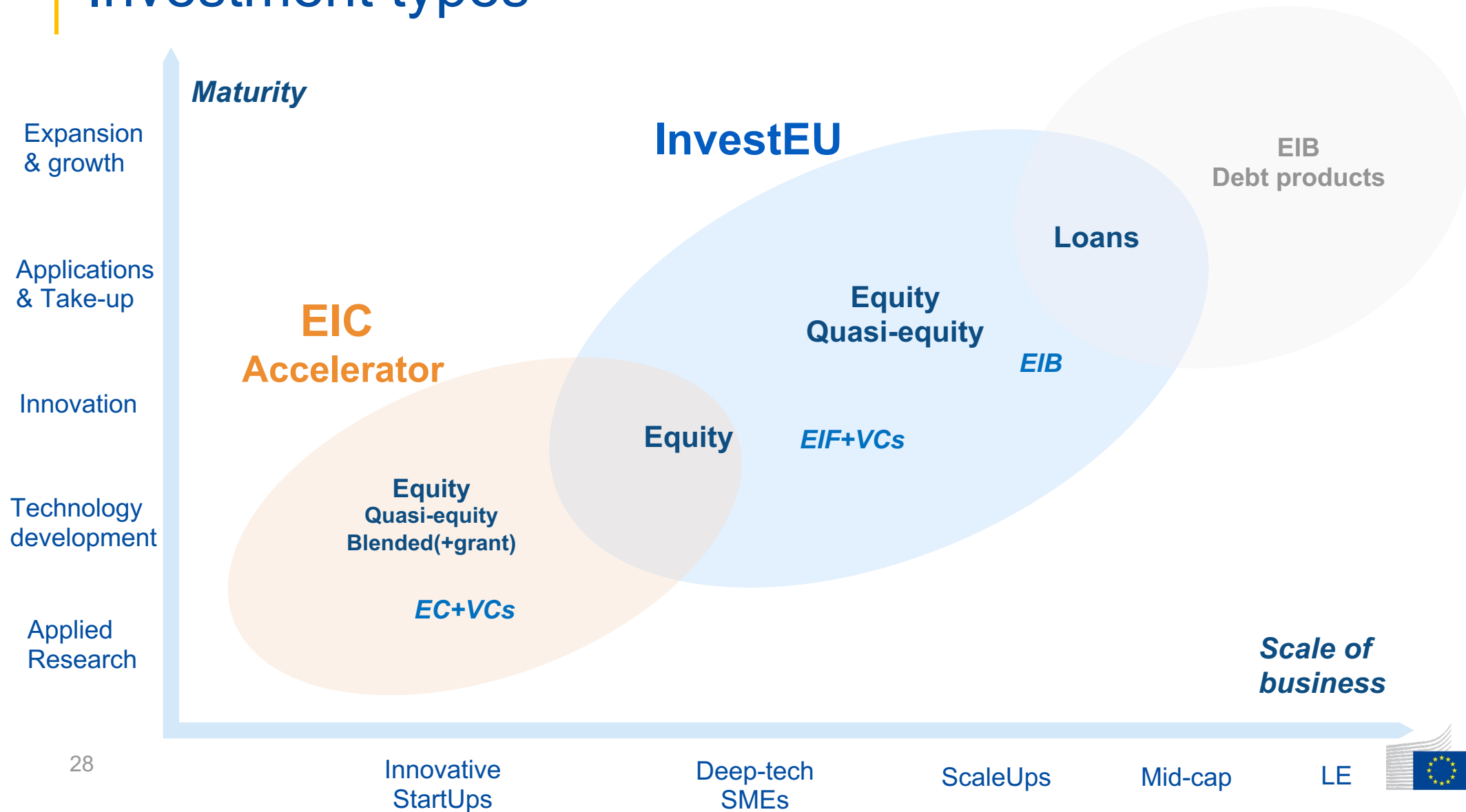


* The “Chips Fund” will be implemented through an investment facility Fund and eligibility criteria are in current EIB group mandates

** An MOU between EIB and EC for investments in semiconductors has been signed upon the Chips Act presentation (8/2/22)

Chips Fund

Investment types

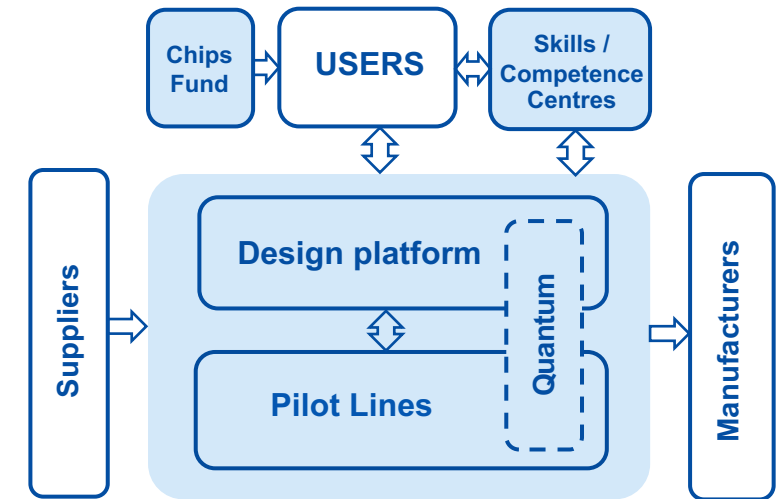


Chips for Europe Initiative

Getting Involved

- **Feb 21:** workshop on **Competence Centres** with Participating States
- **End March:** workshop on **Competence Centres** with users
- **14 March:** online workshop on **Trusted Electronics** (registration at https://ec.europa.eu/eusurvey/runner/Trusted_electronics_Registration_2023)
- **April:** event with investors on **Chips Fund** in collaboration with EIB group
- *Date tbc:* workshop on “**Quantum** in the Chips Act”

Future events (e.g. consultations on pilot lines and design platform) will be disseminated through KDT JU and Industry Associations, also announced on the **digital strategy website**: <https://digital-strategy.ec.europa.eu/>



Inputs and suggestions:

marco.ceccarelli@ec.europa.eu

francisco.ibanez@ec.europa.eu

Thank you

Marco Ceccarelli
Francisco Ibanez



© European Union 2023

Unless otherwise noted the reuse of this presentation is authorised under the [CC BY 4.0](https://creativecommons.org/licenses/by/4.0/) license. For any use or reproduction of elements that are not owned by the EU, permission may need to be sought directly from the respective right holders.

